LM1851

Ground Fault Interrupter

Features

- No potentiometer required
- Direct interface to SCR
- Supply voltage derived from AC line—26V shunt
- Adjustable sensitivity
- Grounded neutral fault detection
- Meets UL943 standards
- 450 μA quiescent current
- Ideal for 120V or 220V systems

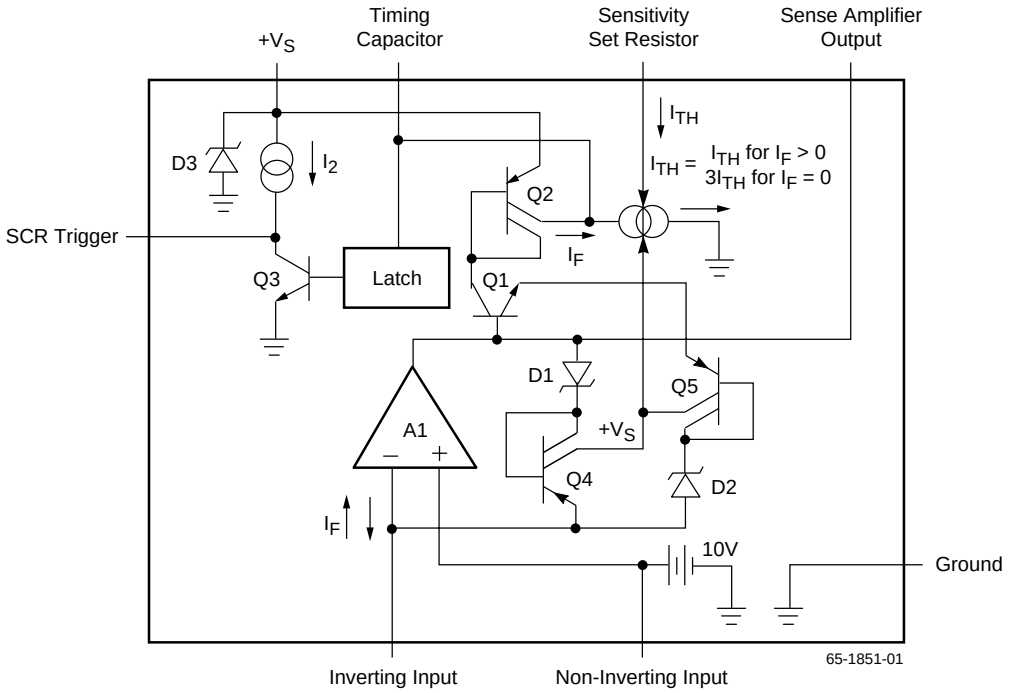
Description

The LM1851 is a controller for AC outlet ground fault interrupters. These devices detect hazardous grounding conditions (example: a pool of water and electrical equipment connected to opposite phases of the AC line) in consumer and industrial environments. The output of the IC triggers an external SCR, which in turn opens a relay circuit breaker to prevent a harmful or lethal shock.

Full advantage of the U.S. UL943 timing specification is taken to ensure maximum immunity to false triggering due to line noise. A special feature is found in circuitry that rapidly resets the integrating timing capacitor in the event that noise pulses introduce unwanted charging currents. Also, flip-flop is included that ensures firing of even a slow circuit breaker relay on either half-cycle of the line voltage when external full wave rectification is used.

The application circuit can be configured to detect both normal faults (hot wire to ground) and grounded neutral faults.

Block Diagram



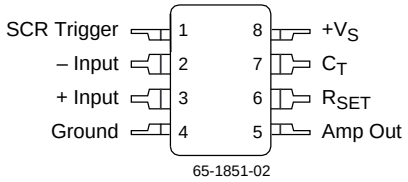
Functional Description

The voltage at the supply pin is clamped to +26V by the internal shunt regulator D3. This shunt regulator also generates an artificial ground voltage for the noninverting input of A1 (shown as a +10V source). A1, Q1, and Q2 act a a current mirror for fault current signals (which are derived from an external transformer). When a fault signal is present, the mirrored current charges the external timing capacitor until its voltage exceeds the latch trigger threshold (typically 17.5V). When then this threshold is exceeded, the latch engages and Q3 turns off, allowing I_2 to drive the SCR connected to pin 1.

Extra Circuitry in the feedback path of A1 works with the switched current source I_1 to remove any charge on C_T induced by noise in the transformer. If no fault current is present, then I_1 discharges C_T with a current equal to 3 I_{TH}, where I_{TH} is the value of current set by the external R_{SET} resistor. If fault signals are present at the input of A1 (which is held at virtual ground, +10V), one of the two current mirrors in the feedback path of A1 (Q4 and Q5) will become active, depending on which half-cycle the fault occurs. This action will raise the voltage at V_S, switching I_1 to a value equal to I_{TH}, and reducing the discharge rate of C_T to better allow fault currents to charge it.

Notice that I_{TH} discharges C_T during both half-cycles of the line, while I_F only charges C_T during the half-cycle in which I_F exits pin 2 (since Q1 will only carry fault current in one direction). Thus, during one half-cycle, I_F-I_{TH} charges C_T, while during the other half-cycle I_{TH} discharges it.

Pin Assignments



Definition of Terms

Normal Fault

An unintentional electrical path, R_B, between the load terminal of the hot line and the ground, as shown by the dashed lines in Figure1.

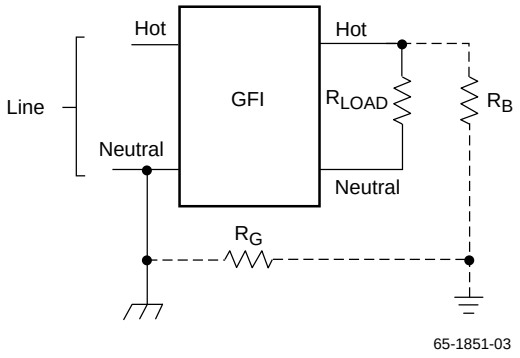


Figure 1. Normal Fault

Grounded Neutral Fault

An unintentional electrical path between the load terminal of the neutral line and the ground, as shown by the dashed lines in Figure 2.

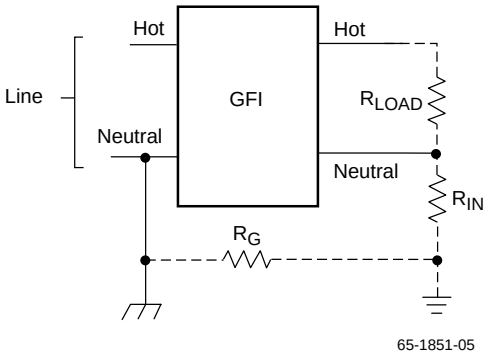


Figure 2. Grounded Neutral Fault

Normal Fault Plus Grounded Neutral Fault

The combination of the normal fault and the grounded neutral fault, as shown by the dashed lines in Figure 3.

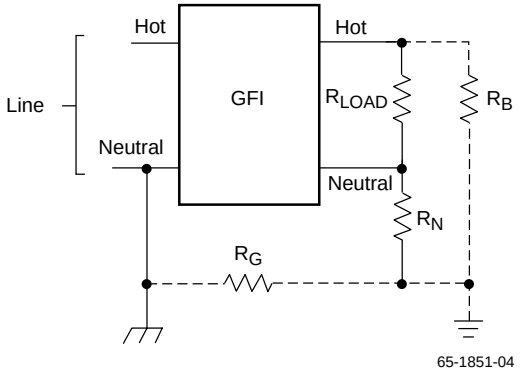


Figure 3. Normal Fault Plus Grounded Neutral Fault

Absolute Maximum Ratings

Parameter	Conditions	Min	Max	Units
Supply Current			19	mA
Power Dissipation			570	mW
Operating Temperature		-40	70	°C
Lead Soldering Temperature	SOIC, 10 seconds		260	°C
	DIP, 60 seconds		300	°C

Thermal Characteristics

Parameter	Conditions	Min	Max	Units
Maximum Junction Temperature			125	°C
Maximum $P_D T_A$ < 50°C	DIP		468	mW
	SOIC		300	
Thermal Resistance, θ_{JA}	DIP		160	°C/W
	SOIC		240	
For TA > 50°C, derate at	DIP		6.25	mW/°C
	SOIC		4.17	

DC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Test Conditions	Min	Typ	Max	Units
Power Supply Shunt Regulator Voltage	Pin 8, Average Value	22	26	30	V
Latch Trigger Voltage	Pin 7	15	17.5	20	V
Sensitivity Set Voltage	Pin 8 to Pin 6	6	7	8.2	V
Output Drive Current	Pin 1 With Fault	0.5	1	2.4	mA
Output Saturation Voltage	Pin 1 Without Fault		100	240	mV
Output Saturation Resistance	Pin 1 Without Fault		100		Ω
Output External Current Sinking Capability[1]	Pin 1 Without Fault, V_{PIN1} Held to 0.3V	2	5		mA
Noise Integration Sink Current Ratio	Pin 7, Ratio of Discharge Currents Between No Fault Fault and Fault Conditions	2.0	2.8	3.6	μA/μA

Notes:

1. This external applied current is in addition to the internal “output drive current” source.

AC Electrical Characteristics

(T_A = +25°C, I_{SHUNT} = 5 mA)

Parameters	Conditions	Min	Typ	Max	Units
Normal Fault Current Sensitivity[2]	See Figure 9	3	5	7	mA
Normal Fault Trip Time[1]	500Ω Fault, see Figure 10		18		mS
Normal Fault With Grounded	500Ω Normal Fault		18		mS
Neutral Fault Trip Time[1]	2Ω Neutral, see Figure 10				

Notes:

1. Average of 10 trials.
2. Required UL sensitivity tolerance is such that external trimming of LM1851 sensitivity is necessary.

Typical Performance Characteristics (T_A = +25°C)

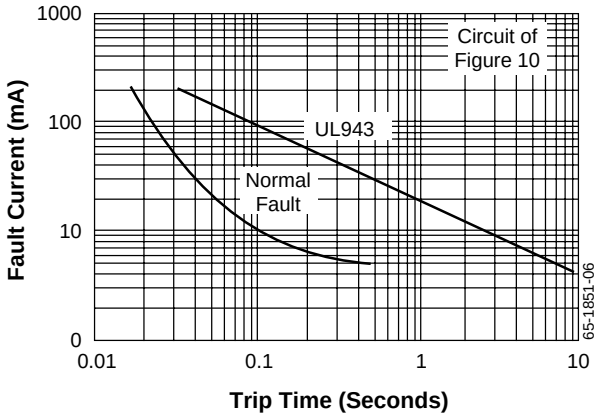


Figure 4. Average Trip Time vs. Fault Current

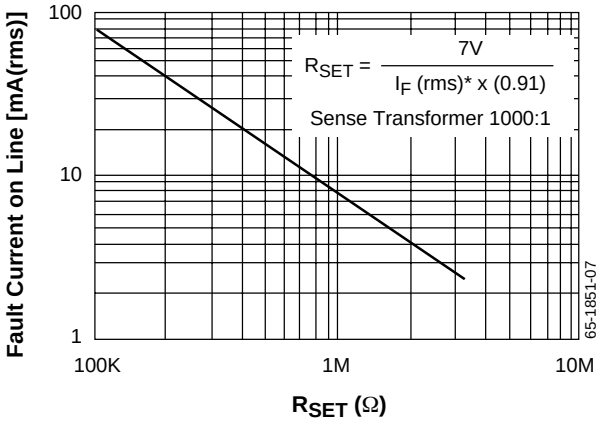


Figure 5. Normal Fault Current Threshold vs. R_{SET}

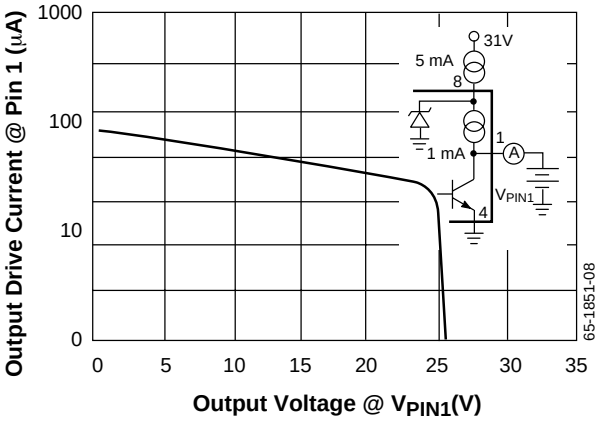


Figure 6. Output Drive Current vs. Output Voltage

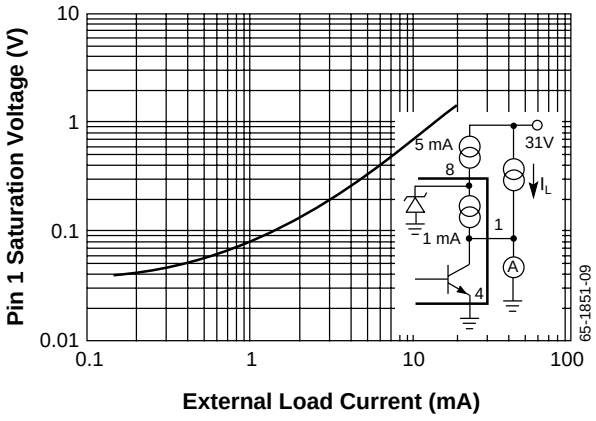


Figure 7. Pin 1 Saturation Voltage vs. External Load Current, I_L

Applications Discussion

A typical ground fault interrupter circuit is shown in Figure 10. It is designed to operate on 120 VAC line voltage with 5 mA normal fault sensitivity.

A full-wave rectifier bridge and a 15k/2W resistor are used to supply the dc power required by the IC. A 1 μF capacitor at pin 8 is used to filter the ripple of the supply voltage and is also connected across the SCR to allow firing of the SCR on either half-cycle. When a fault causes the SCR to trigger, the circuit breaker is energized and line voltage is removed from the load.

At this time no fault current flows and the C_T discharge current increases from I_{TH} to $3I_{TH}$ (see Block Diagram). This quickly resets both the timing capacitor and the output latch. The circuit breaker can be reset and the line voltage again supplied to the load, assuming the fault has been removed. A 1000:1 sense transformer is used to detect the normal fault. The fault current, which is basically the difference current between the got and neutral lines, is stepped down by 1000 and fed into the input pin of the operational amplifier through a 10 μF capacitor. The 0.0033 μF capacitor between pin 2 and pin 3 and the 200 pF between pins 3 and 4 are added to obtain better noise immunity. The normal fault sensitivity is determined by the timing capacitor discharging current, I_{TH}. I_{TH} can be calculated by:

$$I_{TH} = \frac{7V}{R_{SET}} \div 2 \quad (1)$$

At the decision point, the average fault current just equals the threshold current, I_{TH}.

$$I_{TH} = \frac{I_F(rms)}{2} \times 0.91 \quad (2)$$

Where $I_F(rms)$ is the rms input fault current to the operational amplifier and the factor of 2 is due to the fact that I_F charges the timing capacitor only during one half-cycle, while I_{TH} discharges the capacitor continuously. The factor 0.91 converts the rms value to an average value. Combining equations (1) and (2) we have:

$$R_{SET} = \frac{7V}{I_F(rms) \times 0.91} \quad (3)$$

For example, to obtain 5 mA(rms) sensitivity for the circuit in Figure 7 we have:

$$R_{SET} = \frac{7V}{\frac{5\,mA \times 0.91}{1000}} = 1.5M\Omega \quad (4)$$

The correct value for R_{SET} can also be determined from the characteristic curve that plots equation (3). Note that this is an approximate calculation; the exact value of R_{SET} depends on the specific sense transformer used and LM1851 tolerances. Inasmuch as UL943 specifies a sensitivity "window" of 4 mA to 6mA, provision should be made to adjust R_{SET} with a potentiometer.

Independent of setting sensitivity, the desired integration time can be obtained through proper selection of the timing capacitor, C_T. Due to the large number of variables involved, proper selection of C_T is best done empirically. The following design example should only be used as a guideline.

Assume the goal is to meet UL943 timing requirements. Also assume that worst case timing occurs during GFI start-up (S1 closure) with both a heavy normal fault and a 2Ω grounded neutral fault present. This situation is shown diagrammatically in Figure 8.

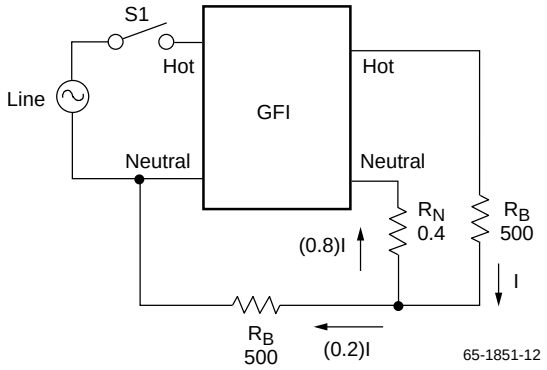


Figure 8.

UL943 specifies ≤25 ms average trip time under these conditions. Calculation of C_T based upon charging currents due to normal fault only is as follows:

1. Start with a ≤25 ms specification. Subtract 3 ms GFI turn-on time (15k and 1 μF). Subtract 8 ms potential loss of one half-cycle due to fault current sense of half-cycles only.

2. Subtract 4 ms time required to open a sluggish circuit breaker.

3. This gives a total ≤10 ms maximum integration time that could be allowed.

4. To generate 8 ms value of integration time that accommodates component tolerances and other variables:

$$C_T = \frac{1 \times T}{V} \quad (5)$$

where:
T = integration time
V = threshold voltage
I = average fault current into CT

$$I = \underbrace{\left(\frac{120\ V_{AC}(rms)}{R_B}\right)}_{\text{heavy fault current generated (swamps } I_{TH})} \quad \underbrace{\left(\frac{RN}{RG + RN}\right)}_{\text{portion of fault current shunted around GFI}}$$

$$\times \underbrace{\left(\frac{1\ \text{turn}}{1000\ \text{turns}}\right)}_{\text{current division of input sense transformer}} \times \underbrace{\left(\frac{1}{2}\right)}_{\text{CT charging on half-cycles only}} \times \underbrace{(0.91)}_{\text{rms to average conversion}} \qquad (6)$$

therefore:

$$C_T = \frac{\left[\left(\frac{120}{500}\right) \times \left(\frac{0.4}{1.6 + 0.4}\right) \times \left(\frac{1}{1000}\right) \times \left(\frac{1}{2}\right) \times (0.91)\right]}{17.5} \times 0.008$$

$$C_T = 0.01\ \mu F \qquad (7)$$

In practice, the actual value of C_T will have to be modified to include the effects of the neutral loop upon the net charging current. The effect of neutral loop induced currents is difficult to quantize, but typically they sum with normal fault currents, thus allowing a larger value of C_T.

For UL943 requirements, 0.015 μF has been found to be the best compromise between timing and noise.

For those GFI standards not requiring grounded neutral detection, a still larger value capacity can be used and better noise immunity obtained.

The larger capacitor can be accommodated because R_N and R_G are not present, allowing the full fault current, I, to enter the GFI.

In Figure 10, grounded neutral detection is accomplished by feeding the neutral coil with 120 Hz energy continuously and allowing some of the energy to couple into the sense transformer during conditions of neutral fault.

Transformers may be obtained from Magnetic Metals, Inc., 21st Street and Hayes Street, Camden, NJ 08101—(609) 964-7842.

Application Circuits

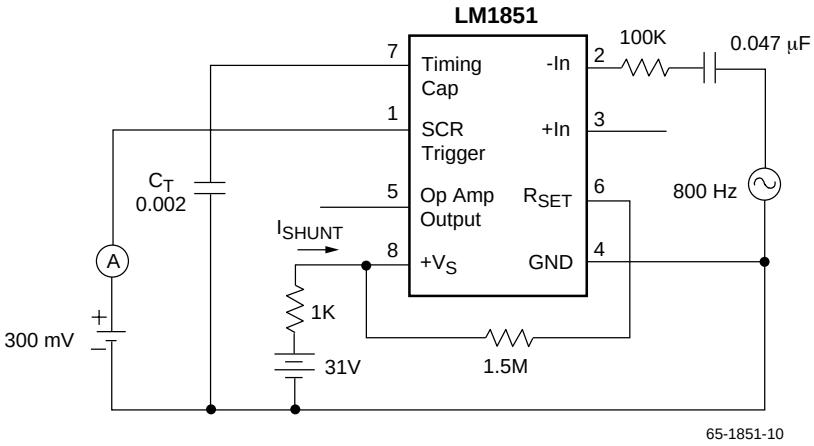
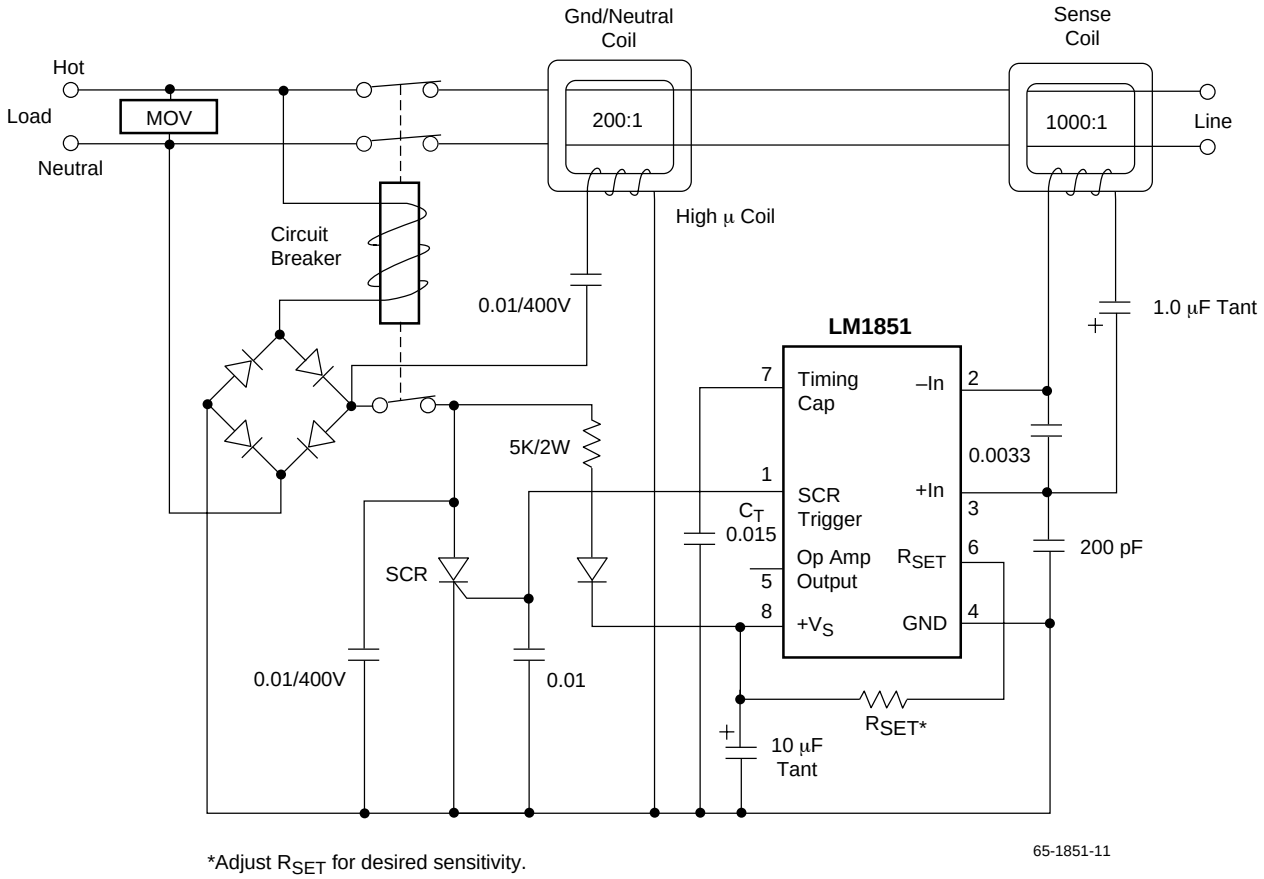


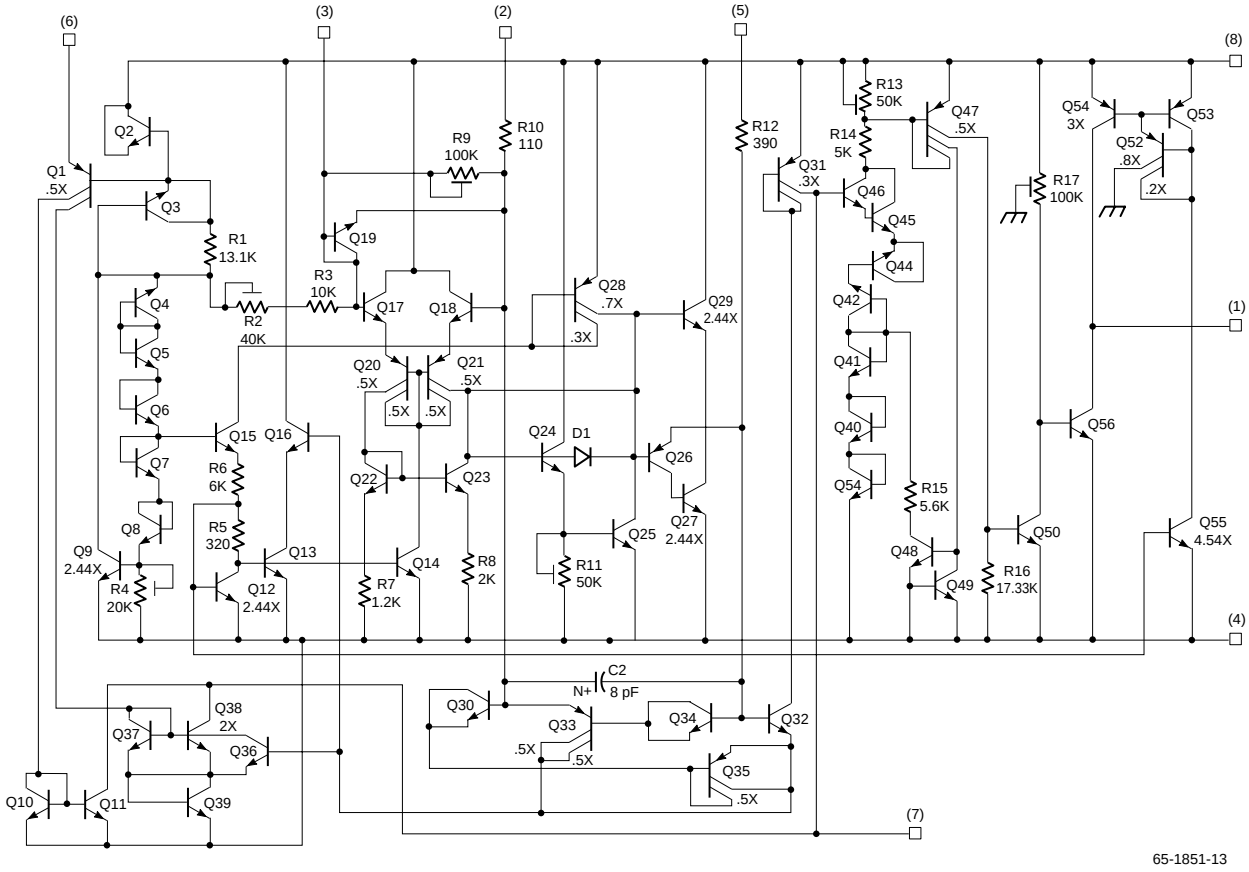
Figure 9. Normal Fault Sensitivity Test Circuit



*Adjust R_{SET} for desired sensitivity.

Figure 10. 120 Hz Neutral Transformer Application

Schematic Diagram



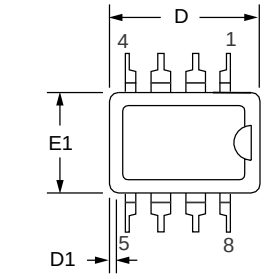
Mechanical Dimensions

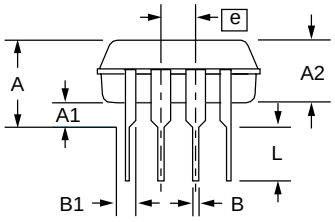
8-Lead Plastic DIP Package

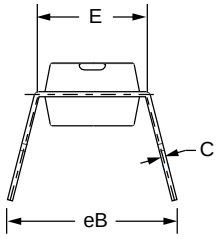
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	—	.210	—	5.33	
A1	.015	—	.38	—	
A2	.115	.195	2.93	4.95	
B	.014	.022	.36	.56	
B1	.045	.070	1.14	1.78	
C	.008	.015	.20	.38	4
D	.348	.430	8.84	10.92	2
D1	.005	—	.13	—	
E	.300	.325	7.62	8.26	
E1	.240	.280	6.10	7.11	2
e	.100 BSC		2.54 BSC		
eB	—	.430	—	10.92	
L	.115	.160	2.92	4.06	
N	8°		8°		5

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E1" do not include mold flashing. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. Terminal numbers are for reference only.
4. "C" dimension does not include solder finish thickness.
5. Symbol "N" is the maximum number of terminals.







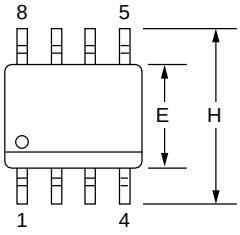
Mechanical Dimensions (continued)

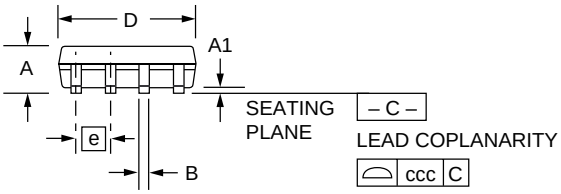
8-Lead Plastic SOIC Package

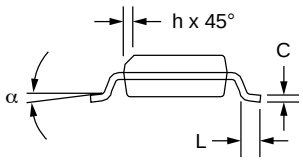
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.053	.069	1.35	1.75	
A1	.004	.010	0.10	0.25	
B	.013	.020	0.33	0.51	
C	.008	.010	0.20	0.25	5
D	.189	.197	4.80	5.00	2
E	.150	.158	3.81	4.01	2
e	.050 BSC		1.27 BSC		
H	.228	.244	5.79	6.20	
h	.010	.020	0.25	0.50	
L	.016	.050	0.40	1.27	3
N	8		8		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Ordering Information

Part Number	Package	Operating Temperature Range
LM1851AN	8-lead Plastic DIP	-40°C to +70°C
RV4145M	8-lead Plastic SOIC	-40°C to +70°C

5/20/98 0.0m 001
Stock#DS30001851