

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

General Description

The EXCLUSIVE-OR gates are monolithic complementary MOS (CMOS) integrated circuits constructed with N- and P-channel enhancement mode transistors. All inputs are protected against static discharge with diodes to V_{DD} and V_{SS} .

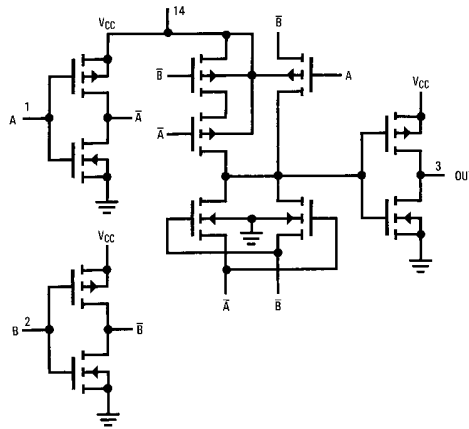
Features

- Wide supply voltage range 3.0V to 15V
- Low power 100 nW (typ.)
- Medium speed operation $t_{PHL} = t_{PLH} = 40$ ns (typ.)
at $C_L = 15$ pF, 10V supply
- High noise immunity 0.45 V_{CC} (typ.)

Applications

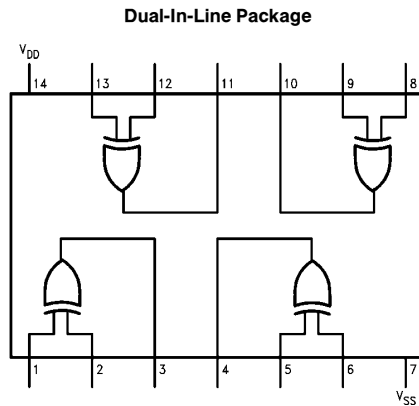
- Automotive
- Data terminals
- Instrumentation
- Medical electronics
- Industrial controls
- Remote metering
- Computers

Schematic Diagram



TL/F/5961-1

Connection Diagram



TL/F/5961-2

Order Number CD4030

CD4030M/CD4030C Quad EXCLUSIVE-OR Gate

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Voltage at Any Pin (Note 1) $V_{SS} - 0.3V$ to $V_{SS} + 15.5V$
 Operating Temperature Range
 CD4030M $-55^{\circ}C$ to $+125^{\circ}C$
 CD4030C $-40^{\circ}C$ to $+85^{\circ}C$

Storage Temperature Range $-65^{\circ}C$ to $+150^{\circ}C$
 Power Dissipation (P_D)
 Dual-In-Line 700 mW
 Small Outline 500 mW
 Operating V_{DD} Range $V_{SS} + 3.0V$ to $V_{SS} + 15V$
 Lead Temperature
 (Soldering, 10 seconds) $260^{\circ}C$

DC Electrical Characteristics CD4030M

Symbol	Parameter	Conditions	Limits									Units
			$-55^{\circ}C$			$+25^{\circ}C$			$+125^{\circ}C$			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.5		0.005	0.5			30	μA
					1.0		0.01	1.0			60	μA
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$			2.5		0.025	2.5			150	μW
					10		0.1	10			600	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05		0	0.05			0.05	V
					0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$	4.95			4.95	5.0		4.95			V
			9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.5			1.5	2.25		1.4			V
			3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.4			1.5	2.25		1.5			V
			2.9			3.0	4.5		3.0			V
I_{DN}	Output Drive Current N-Channel (Note 2)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	0.75			0.6	1.2		0.45			mA
			1.5			1.2	2.4		0.9			mA
I_{DP}	Output Drive Current P-Channel (Note 2)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	-0.45			-0.3	-0.6		-0.21			mA
			-0.95			-0.65	-1.3		-0.45			mA
I_I	Input Current	$V_I = 0V$ or $V_I = V_{DD}$					10				pA	

DC Electrical Characteristics CD4030C

Symbol	Parameter	Conditions	Limits									Units
			$-40^{\circ}C$			$+25^{\circ}C$			$+85^{\circ}C$			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
I_L	Quiescent Device Current	$V_{DD} = 5.0V$ $V_{DD} = 10V$			5.0		0.05	5.0			70	μA
					10		0.1	10			140	μA
P_D	Quiescent Device Dissipation Package	$V_{DD} = 5.0V$ $V_{DD} = 10V$			25		0.25	25			350	μW
					100		1.0	100			1,400	μW
V_{OL}	Output Voltage Low Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$			0.05		0	0.05			0.05	V
					0.05		0	0.05			0.05	V
V_{OH}	Output Voltage High Level	$V_{DD} = 5.0V$ $V_{DD} = 10V$	4.95			4.95	5.0		4.95			V
			9.95			9.95	10		9.95			V
V_{NL}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.5			1.5	2.25		1.4			V
			3.0			3.0	4.5		2.9			V
V_{NH}	Noise Immunity (All Inputs)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	1.4			1.5	2.25		1.5			V
			2.9			3.0	4.5		3.0			V
I_{DN}	Output Drive Current N-Channel (Note 2)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	0.35			0.3	1.2		0.25			mA
			0.7			0.6	2.4		0.5			mA
I_{DP}	Output Drive Current P-Channel (Note 2)	$V_{DD} = 5.0V$ $V_{DD} = 10V$	-0.21			-0.15	-0.6		-0.12			mA
			-0.45			-0.32	-1.3		-0.25			mA
I_I	Input Current	$V_I = 0V$ or $V_I = V_{DD}$					10				pA	

AC Electrical Characteristics* CD4030M

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t _{PHL}	Propagation Delay Time	V _{DD} = 5.0V V _{DD} = 10V		100	200	ns
				40	100	ns
t _{PLH}	Propagation Delay Time	V _{DD} = 5.0V V _{DD} = 10V		100	200	ns
				40	100	ns
t _{THL}	Transition Time High to Low Level	V _{DD} = 5.0V V _{DD} = 10V		70	150	ns
				25	75	ns
t _{TLH}	Transition Time Low to High Level	V _{DD} = 5.0V V _{DD} = 10V		80	150	ns
				30	75	ns
C _I	Input Capacitance	V _I = 0V or V _I = V _{DD}		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

AC Electrical Characteristics* CD4030C

Symbol	Parameter	Conditions	Limits			Units
			Min	Typ	Max	
t _{PHL}	Propagation Delay Time	V _{DD} = 5.0V V _{DD} = 10V		100	300	ns
				40	150	ns
t _{PLH}	Propagation Delay Time	V _{DD} = 5.0V V _{DD} = 10V		100	300	ns
				40	150	ns
t _{THL}	Transition Time High to Low Level	V _{DD} = 5.0V V _{DD} = 10V		70	300	ns
				25	150	ns
t _{TLH}	Transition Time Low to High Level	V _{DD} = 5.0V V _{DD} = 10V		80	300	ns
				30	150	ns
C _I	Input Capacitance	V _I = 0V or V _I = V _{DD}		5.0		pF

*AC Parameters are guaranteed by DC correlated testing.

Note 1: This device should not be connected to circuits with power on because high transient voltages may cause permanent damage.

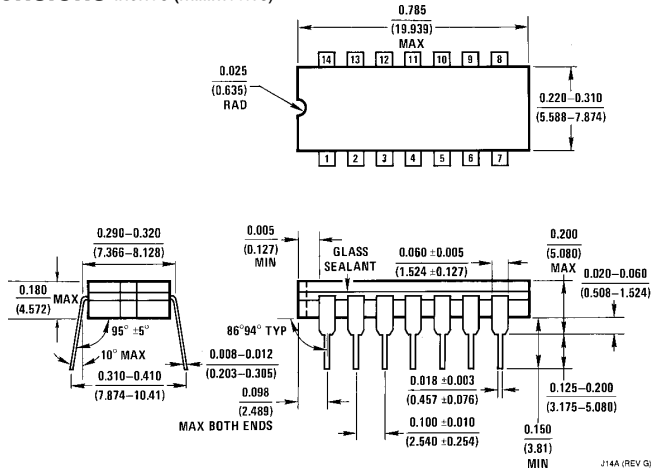
Note 2: I_{DN} and I_{DP} are tested one output at a time.

Truth Table (For One of Four Identical Gates)

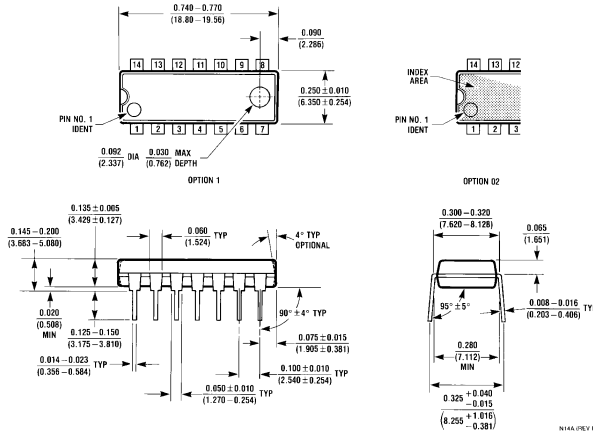
A	B	J
0	0	0
1	0	1
0	1	1
1	1	0

Where: "1" = High Level
"0" = Low Level

Physical Dimensions inches (millimeters)



Ceramic Dual-In-Line Package (J)
Order Number CD4030MJ or CD4030CJ
NS Package Number J14A



Molded Dual-In-Line Package (N)
Order Number CD4030MN or CD4030CN
NS Package Number N14A

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