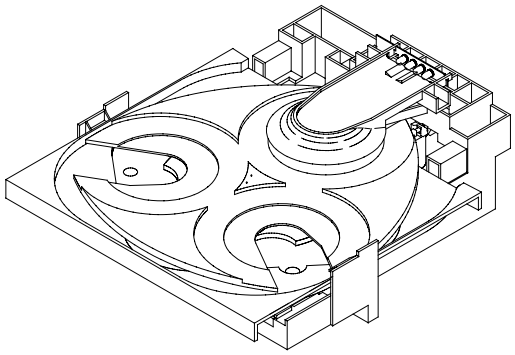
aiwa SERVICE

4ZG-1

English



SERVICE MANUAL

CD MECHANISM

BASIC CD MECHANISM : 3ZG-2 E3
KSM-2131 FAM

TYPE	BASIC CD MECHANISM
VOS1NDSHM	3ZG-2 E3
VOS1RNDSM	3ZG-2 E3
VOS1RMDSM	3ZG-2 E3
VOS1RMDS	KSM-2131 FAM
VOS1RNDSC	KSM-2131 FAM

aiwa

S/M Code No. 09-992-325-4N8

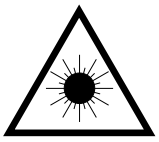
DATA

PROTECTION OF EYES FROM LASER BEAM DURING SERVICING

This set employs laser. Therefore, be sure to follow carefully the instructions below when servicing.

WARNING!

WHEN SERVICING, DO NOT APPROACH THE LASER EXIT WITH THE EYE TOO CLOSELY. IN CASE IT IS NECESSARY TO CONFIRM LASER BEAM EMISSION. BE SURE TO OBSERVE FROM A DISTANCE OF MORE THAN 30cm FROM THE SURFACE OF THE OBJECTIVE LENS ON THE OPTICAL PICK-UP BLOCK.



- Caution: Invisible laser radiation when open and interlocks defeated avoid exposure to beam.
- Advarsel: Usynling laserstråling ved åbning, når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

VAROITUS!

Laiteen Käyttäminen muulla kuin tässä käyttöohjeessa mainitulla tavalla saattaa altistaa käyt-täjän turvallisuusluokan 1 ylittävälle näkymättömälle lasersäteilylle.

VARNING!

Om apparaten används på annat sätt än vad som specificeras i denna bruksanvising, kan användaren utsättas för osynling laserstrålning, som överskrider gränsen för laserklass 1.

CAUTION

Use of controls or adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

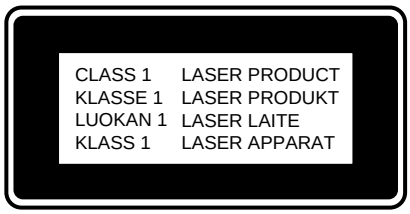
ATTENTION

L'utilisation de commandes, réglages ou procédures autres que ceux spécifiés peut entraîner une dangereuse exposition aux radiations.

ADVARSEL!

Usynlig laserstråling ved åbning, når sikkerhedsafbrydereer ude af funktion. Undgå udsættelse for stråling.

This Compact Disc player is classified as a CLASS 1 LASER product.
The CLASS 1 LASER PRODUCT label is located on the rear exterior.

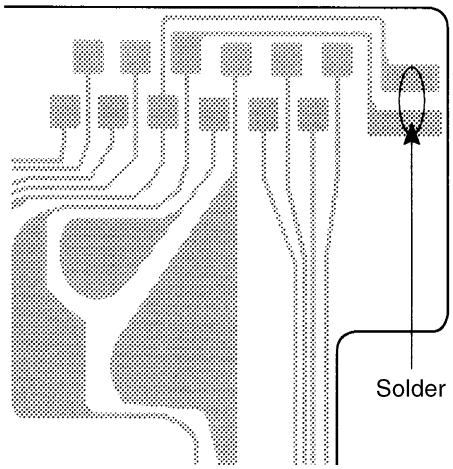


Precaution to replace Optical block (KSS-213F)

Body or clothes electrostatic potential could ruin laser diode in the optical block. Be sure ground body and workbench, and use care the clothes do not touch the diode.

1) After the connection, remove solder shown in the right figure.

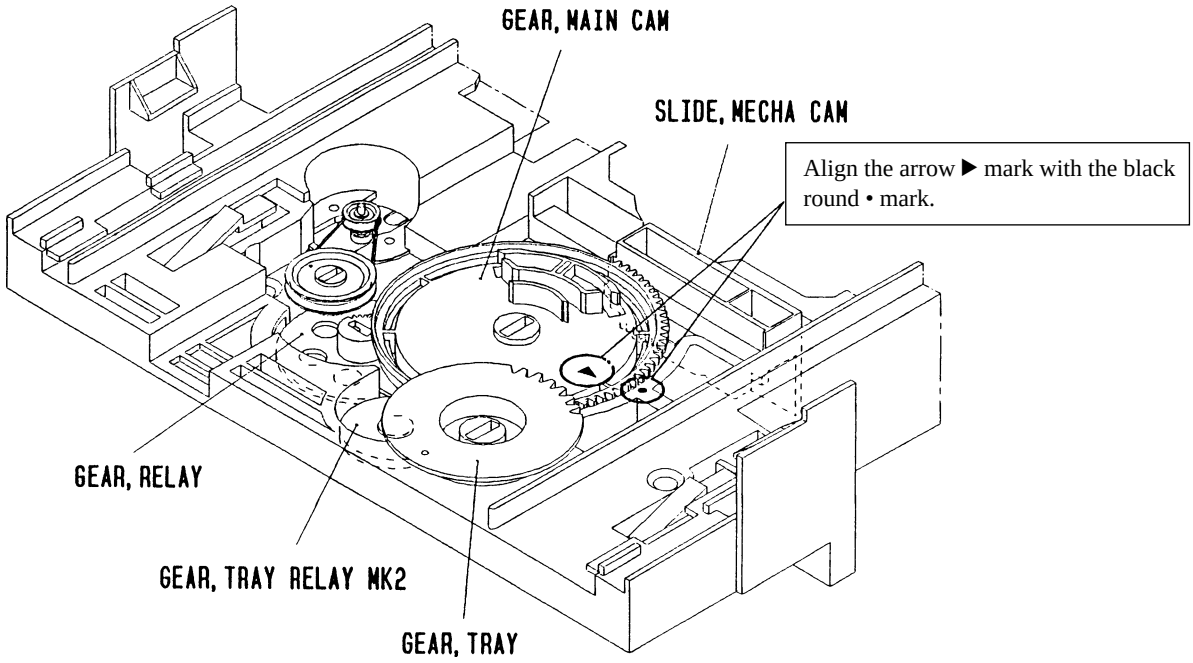
PICK-UP Assy P.C.B



How to Adjust the Rotating Phase of the Gear, Main Cam

1) Push down the hooking catch of the CHAS. MECH, and remove the TRAY.
2) Align the arrow mark of the Gear, Main Cam with the black round mark of the CHAS, MECHA as shown below.
3) Confirm that the Slide, Mech Cam is located in the right position, then insert the TRAY gently.

Caution: If the rotating phase of the Gear, Main Cam is incorrectly adjusted, the chucking operation and tray movement will have malfunction.



ELECTRICAL MAIN PARTS LIST

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
IC			
	87-A20-547-010		C-IC,CXA1992AR
	87-A20-919-040		C-IC,BA5915FP
	87-A20-917-010		C-IC,CXD2540Q-1/2
	84-ZG1-698-010		C-IC,UPD78016FGC-553
	87-017-825-010		IC,GP1F32T
	87-017-760-080		IC,M51943BML
	87-A20-602-040		C-IC,M5291FP
	87-A20-925-040		C-IC,BA05FP
	87-A20-905-040		C-IC,BA033FP
	87-001-873-010		IC,LB1644
	87-A20-920-010		C-IC,CL680-D1
	87-A20-921-040		C-IC,SN74LVU04APW
	87-A20-962-040		C-IC,MSM54V16258B/BSL
	84-ZG1-695-040		C-IC,LH5V2RN1
	87-A20-975-040		C-IC,SN74LV74APW
	87-A20-974-040		C-IC,LC74781M-9017
	87-A20-918-040		C-IC,SM5878AM
TRANSISTOR			
	87-026-463-080		TR,2SA933S (0.3W)
	87-026-237-080		CHIP-TR,DTC124XK
	89-327-125-080		CHIP TR,2SC2712GR
	87-026-231-080		CHIP-TRANSISTER,DTA124XK
	87-A30-288-040		CHIP-TR,DTC114YKA <VOS1RMDSM,VOS1RMDS>
	87-A30-117-010		TR,2SA1357
	89-111-625-080		TR,2SA1162 (0.15W)
	87-026-580-080		C-TR,DTA123JK
	87-026-470-080		TR,HN1C03F (0.3W)
DIODE			
	87-020-027-080		CHIP-DIODE 1SS184
	87-017-024-040		C-DIODE,DA204K
	87-A40-180-040		C-DIODE,SB07-015C
	87-A40-384-080		C-ZENER,UDZ3.3B
VCD C.B			
C101	87-010-182-080		C-CAP,S 2200P-50 B
C102	87-016-669-080		C-CAP,S 0.1-25 K B
C103	87-016-669-080		C-CAP,S 0.1-25 K B
C104	87-016-669-080		C-CAP,S 0.1-25 K B
C105	87-010-404-040		CAP,E 4.7-50 SME
C106	87-016-369-080		C-CAP,S 0.033-25 B K
C107	87-010-197-080		CAP, CHIP 0.01 DM
C108	87-010-401-040		CAP,E 1-50 SME
C109	87-010-382-040		CAP,E 22-25 SME
C110	87-010-213-080		C-CAP,S 0.015-50 B
C111	87-010-263-040		CAP,E 100-10
C112	87-010-197-080		CAP, CHIP 0.01 DM
C113	87-016-369-080		C-CAP,S 0.033-25 B K
C114	87-016-369-080		C-CAP,S 0.033-25 B K
C115	87-016-369-080		C-CAP,S 0.033-25 B K
C116	87-012-158-080		C-CAP,S 390P-50 CH
C117	87-012-154-080		C-CAP,S 150P-50 CH
C118	87-010-494-040		CAP,E 1-50 GAS
C119	87-010-313-080		CAP, CHIP 18P
C120	87-010-992-080		C-CAP,S 0.047-25 B
C121	87-010-992-080		C-CAP,S 0.047-25 B
C123	87-016-669-080		C-CAP,S 0.1-25 K B
C125	87-010-198-080		CAP, CHIP 0.022
C126	87-016-669-080		C-CAP,S 0.1-25 K B
C127	87-010-555-040		CAP,E 100-10 GAS
C130	87-010-555-040		CAP,E 100-10 GAS
C131	87-010-555-040		CAP,E 100-10 GAS
C132	87-010-178-080		CHIP CAP 1000P
C133	87-010-555-040		CAP,E 100-10 GAS
C134	87-010-196-080		CHIP CAPACITOR,0.1-25
C135	87-010-196-080		CHIP CAPACITOR,0.1-25
C136	87-010-196-080		CHIP CAPACITOR,0.1-25
C137	87-010-196-080		CHIP CAPACITOR,0.1-25
C138	87-010-184-080		CHIP CAPACITOR 3300P(K)
C139	87-010-197-080		CAP, CHIP 0.01 DM
C140	87-010-112-040		CAP,E 100-16
C141	87-010-196-080		CHIP CAPACITOR,0.1-25
C142	87-010-196-080		CHIP CAPACITOR,0.1-25
C143	87-010-213-080		C-CAP,S 0.015-50 B
C151	87-010-263-040		CAP,E 100-10
C152	87-010-197-080		CAP, CHIP 0.01 DM
C153	87-A10-893-040		CAP,E 220-10 M PW
C154	87-010-190-080		S CHIP F 0.01
C155	87-010-184-080		CHIP CAPACITOR 3300P(K)
C156	87-010-992-080		C-CAP,S 0.047-25 B
C157	87-010-992-080		C-CAP,S 0.047-25 B
C158	87-012-156-080		C-CAP,S 220P-50 CH
C159	87-016-526-080		C-CAP,S 0.47-16 BK
C160	87-010-314-080		C-CAP,S 22P-50V
C161	87-010-182-080		C-CAP,S 2200P-50 B
C162	87-010-178-080		CHIP CAP 1000P
C201	87-016-669-080		C-CAP,S 0.1-25 K B
C204	87-010-190-080		S CHIP F 0.01
C205	87-010-379-040		CAP,E 22-16 M SME
C206	87-010-322-080		C-CAP,S 100P-50 CH
C207	87-010-322-080		C-CAP,S 100P-50 CH
C208	87-010-322-080		C-CAP,S 100P-50 CH
C209	87-010-322-080		C-CAP,S 100P-50 CH
C210	87-016-669-080		C-CAP,S 0.1-25 K B
C211	87-010-263-040		CAP,E 100-10
C213	87-010-190-080		S CHIP F 0.01
C214	87-010-196-080		CHIP CAPACITOR,0.1-25
C301	87-016-251-040		CAP,E 220-16 SMG
C302	87-012-140-080		CAP 470P
C303	87-010-178-080		CHIP CAP 1000P
C304	87-010-384-040		CAP,E 100-25 SME
C305	87-010-982-040		CAP,E 33-25 GAS
C306	87-010-112-040		CAP,E 100-16
C307	87-010-196-080		CHIP CAPACITOR,0.1-25
C308	87-010-263-040		CAP,E 100-10
C309	87-010-196-080		CHIP CAPACITOR,0.1-25
C310	87-010-263-040		CAP,E 100-10
C311	87-010-196-080		CHIP CAPACITOR,0.1-25
C312	87-010-178-080		CHIP CAP 1000P
C320	87-010-196-080		CHIP CAPACITOR,0.1-25
C401	87-016-044-040		CAP,E 100-16 GAS
C402	87-010-190-080		S CHIP F 0.01
C403	87-010-190-080		S CHIP F 0.01
C404	87-010-552-040		CAP,E 22-16 GAS
C501	87-010-197-080		CAP, CHIP 0.01 DM
C502	87-010-197-080		CAP, CHIP 0.01 DM
C503	87-010-197-080		CAP, CHIP 0.01 DM
C504	87-010-154-080		CAP CHIP 10P
C505	87-010-154-080		CAP CHIP 10P
C506	87-010-197-080		CAP, CHIP 0.01 DM
C508	87-010-263-040		CAP,E 100-10
C509	87-016-669-080		C-CAP,S 0.1-25 K B
C510	87-010-263-040		CAP,E 100-10
C511	87-010-196-080		CHIP CAPACITOR,0.1-25
C512	87-010-197-080		CAP, CHIP 0.01 DM
C513	87-010-197-080		CAP, CHIP 0.01 DM
C514	87-010-197-080		CAP, CHIP 0.01 DM
C518	87-010-322-080		C-CAP,S 100P-50 CH
C519	87-012-145-080		CAP, CHIP S 270P CH
C520	87-012-157-080		C-CAP,S 330P-50 CH
C521	87-012-154-080		C-CAP,S 150P-50 CH
C522	87-010-371-080		CAP, ELECT 470-6.3V
C523	87-010-197-080		CAP, CHIP 0.01 DM
C524	87-010-197-080		CAP, CHIP 0.01 DM

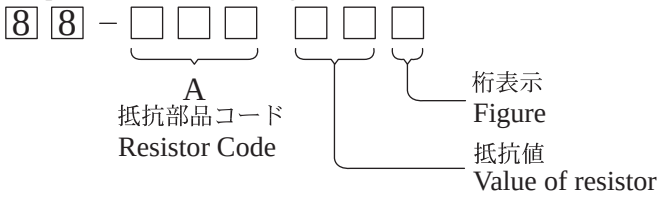
REF. NO	PART NO.	KANRI NO.	DESCRIPTION
C525	87-010-197-080		CAP, CHIP 0.01 DM
C526	87-010-197-080		CAP, CHIP 0.01 DM
C527	87-010-197-080		CAP, CHIP 0.01 DM
C528	87-010-197-080		CAP, CHIP 0.01 DM
C529	87-010-197-080		CAP, CHIP 0.01 DM
C530	87-010-197-080		CAP, CHIP 0.01 DM
C531	87-010-197-080		CAP, CHIP 0.01 DM
C532	87-010-374-040		CAP,E 47-10
C533	87-010-197-080		CAP, CHIP 0.01 DM
C534	87-010-555-040		CAP,E 100-10 GAS
C535	87-010-197-080		CAP, CHIP 0.01 DM
C536	87-010-078-040		CAP,E 47-6.3 5L
C537	87-010-190-080		S CHIP F 0.01
C538	87-010-196-080		CHIP CAPACITOR,0.1-25
C539	87-010-196-080		CHIP CAPACITOR,0.1-25
C540	87-010-078-040		CAP,E 47-6.3 5L
C541	87-010-197-080		CAP, CHIP 0.01 DM
C542	87-010-318-080		C-CAP,S 47P-50 CH
C544	87-010-197-080		CAP, CHIP 0.01 DM
C546	87-010-197-080		CAP, CHIP 0.01 DM
C549	87-010-494-040		CAP,E 1-50 GAS
C550	87-010-196-080		CHIP CAPACITOR,0.1-25
C551	87-012-153-080		C-CAP,S 120P-50 CH
C552	87-016-526-080		C-CAP,S 0.47-16 BK
C554	87-010-197-080		CAP, CHIP 0.01 DM
C556	87-010-197-080		CAP, CHIP 0.01 DM
C557	87-A11-167-080		C-CAP,S 27P-50 F CH
C558	87-A11-167-080		C-CAP,S 27P-50 F CH
C560	87-010-197-080		CAP, CHIP 0.01 DM
C601	87-010-197-080		CAP, CHIP 0.01 DM
C602	87-010-197-080		CAP, CHIP 0.01 DM
C603	87-010-112-040		CAP,E 100-16
C604	87-010-196-080		CHIP CAPACITOR,0.1-25
C605	87-010-197-080		CAP, CHIP 0.01 DM
C606	87-010-197-080		CAP, CHIP 0.01 DM
C607	87-010-313-080		CAP, CHIP 18P
C608	87-010-313-080		CAP, CHIP 18P
C609	87-010-178-080		CHIP CAP 1000P
C610	87-010-178-080		CHIP CAP 1000P
C611	87-010-178-080		CHIP CAP 1000P
C612	87-010-178-080		CHIP CAP 1000P
C613	87-010-403-040		CAP,E 3.3-50 SME
C614	87-010-403-040		CAP,E 3.3-50 SME
C615	87-010-318-080		C-CAP,S 47P-50 CH
C616	87-010-318-080		C-CAP,S 47P-50 CH
CN101	87-A60-424-010		CONN,16P V TOC-B
CN102	87-099-199-010		CONN,6P 6216 H
CN201	87-009-345-010		CONN,2P PH H<VOS1RMDSM,VOS1RMDS>
CN301	87-099-199-010		CONN,6P 6216 H
CN401	87-099-212-010		CONN,5P 6216 V

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
CN403	87-099-030-010		CONN,13P 6216H
FB201	83-XM1-617-080		C-COIL,BK2125HM601 <VOS1RMDSM,VOS1RMDS>
J501	87-009-502-010		JACK,PIN 1P Y EARTH
L101	87-005-196-080		COIL,10UH
L301	87-A50-095-010		COIL,68UH RCR875D
L302	87-005-426-080		COIL,3.3UH K FLR50
L502	87-005-204-080		COIL,47UH
L503	87-005-189-080		COIL 2.7UH
L504	87-005-187-080		COIL,1.8UH
L505	87-005-204-080		COIL,47UH
L506	87-005-204-080		COIL,47UH
L507	87-005-204-080		COIL,47UH
L508	87-005-817-080		C-COIL, 33UH J FLC32
M601	87-045-305-010		MOTOR, RF-500TB DC-5V (2MA) <EXCEPT VOS1RNDSC>
M601	87-045-383-010		MOT,M9I50T28-2<VOS1RNDSC>
R130	87-022-364-080		C-RES,S 82K-1/10W F
R131	87-022-364-080		C-RES,S 82K-1/10W F
R132	87-022-364-080		C-RES,S 82K-1/10W F
R133	87-022-364-080		C-RES,S 82K-1/10W F
R134	87-022-364-080		C-RES,S 82K-1/10W F
R135	87-022-364-080		C-RES,S 82K-1/10W F
S201	87-A90-162-010		SW,SL 1-1-3 SSSU
S401	87-036-109-010		PUSH SWITCH
S402	87-036-109-010		PUSH SWITCH
FC1	85-NFT-611-110		FF-CABLE 16P-1.0
FC2	84-ZG1-630-010		CABLE FFC 6P-1.25
X201	87-A70-124-080		VIB,CER 8.0MHZ
X501	87-A70-125-080		VIB,XTAL 27MHZ 50PPM
X601	87-030-270-080		VIB,XTAL 16.9344MHZ
LED C.B<VOS1RMDSM,VOS1RMDS>			
LED401	87-A40-447-040		LED,SLP-6130C-81H-S-T1 ORN <VOS1RMDSM,VOS1RMDS>
LED402	87-017-350-080		LED,SEL1550CM<VOS1RMDSM,VOS1RMDS>
LED403	87-017-350-080		LED,SEL1550CM<VOS1RMDSM,VOS1RMDS>
LED404	87-A40-447-040		LED,SLP-6130C-81H-S-T1 ORN <VOS1RMDSM,VOS1RMDS>
T-T C.B			
FC3	84-ZG1-673-010		F-CABLE,5P 1.25 210MM BLACK N
FC3	84-ZG1-672-010		F-CABLE,5P 1.25 210MM WHITE N
C401	87-A11-148-080		CAP,TC U 0.1-50 Z F
CN401	86-NFZ-675-010		CONN,5P H 6216-11H
M401	87-045-364-010		MOTOR(BCH3B14)
PS401	87-026-573-010		IC,GP1S53V

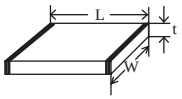
- Regarding connectors, they are not stocked as they are not the initial order items.
  The connectors are available after they are supplied from connector manufacturers upon the order is received.

○チップ抵抗部品コード／CHIP RESISTOR PART CODE

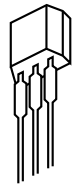
チップ抵抗部品コードの成り立ち
Chip Resistor Part Coding



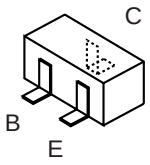
チップ抵抗
Chip resistor

容量 Wattage	種類 Type	許容誤差 Tolerance	記号 Symbol	寸法／Dimensions (mm) 外形／Form	L	W	t	抵抗コード ：A Resistor Code：A
1/16W	1005	±5%	CJ		1.0	0.5	0.35	104
1/16W	1608	±5%	CJ		1.6	0.8	0.45	108
1/10W	2125	±5%	CJ		2	1.25	0.45	118
1/8W	3216	±5%	CJ		3.2	1.6	0.55	128

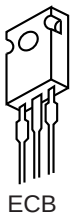
TRANSISTOR ILLUSTRATION



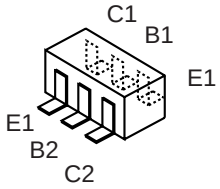
2SA933S



2SA1162
2SC2712
DTA123JK
DTA124XK
DTC114YKA
DTC124XK

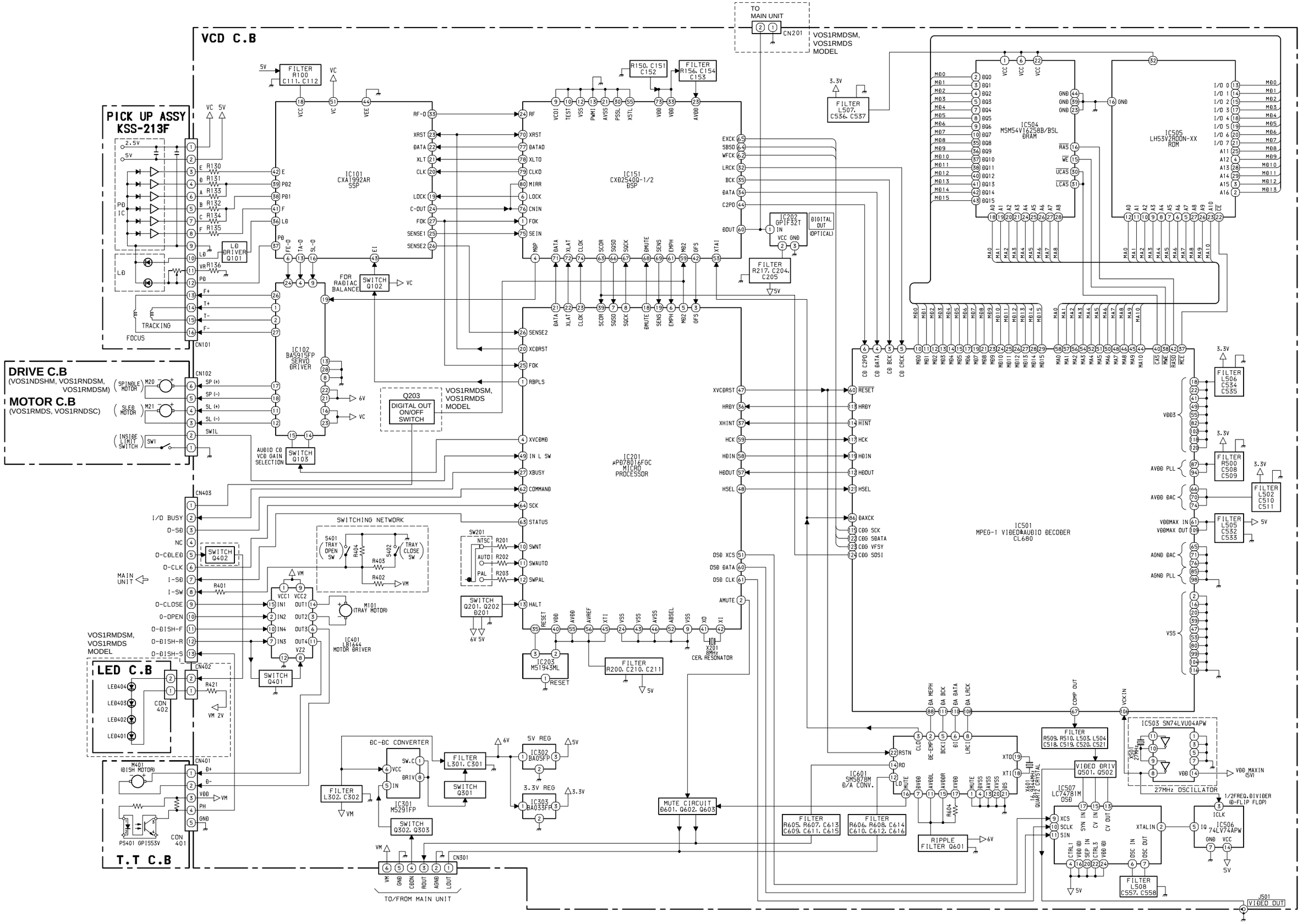


2SA1357

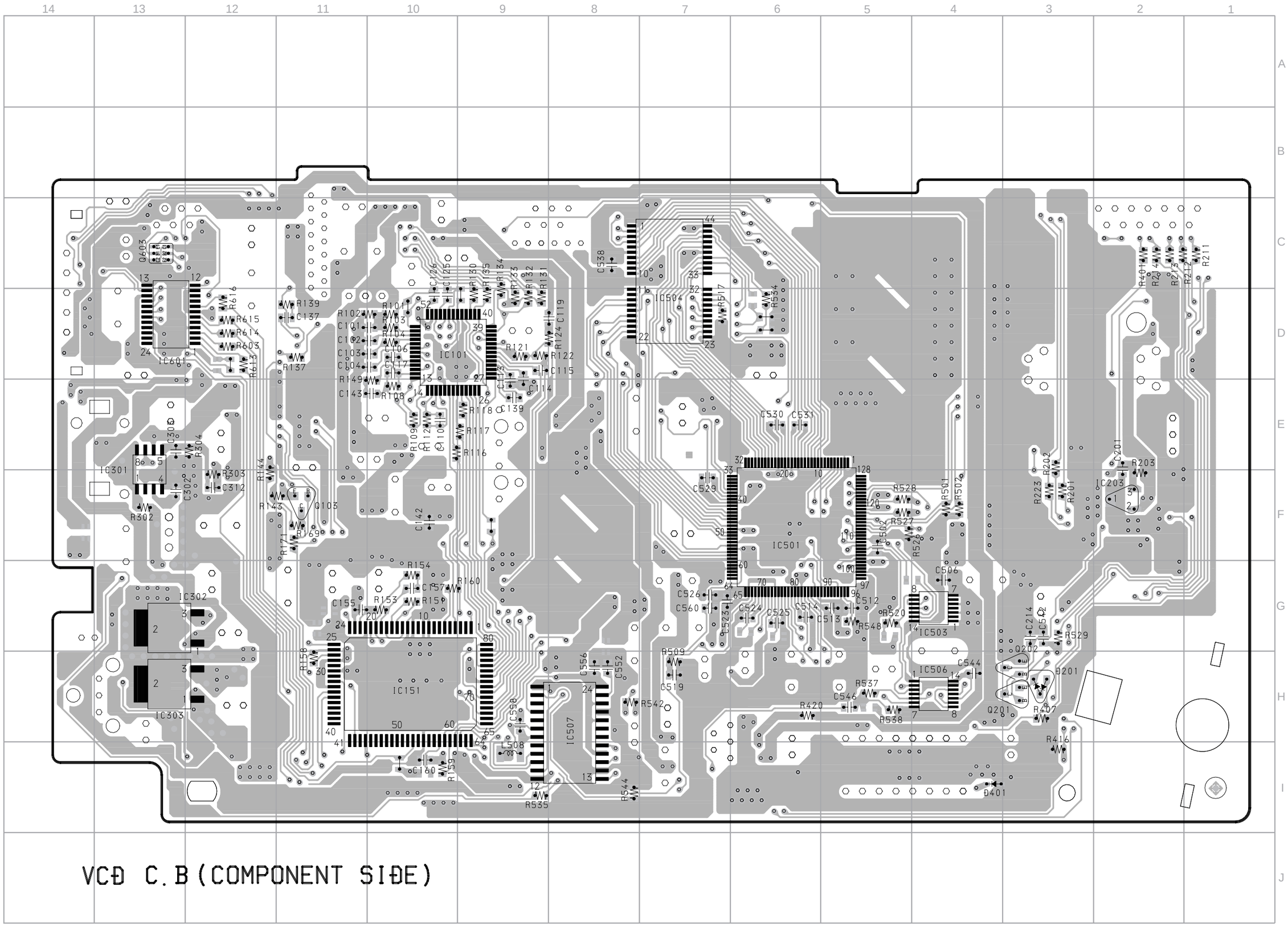


HN1C03F

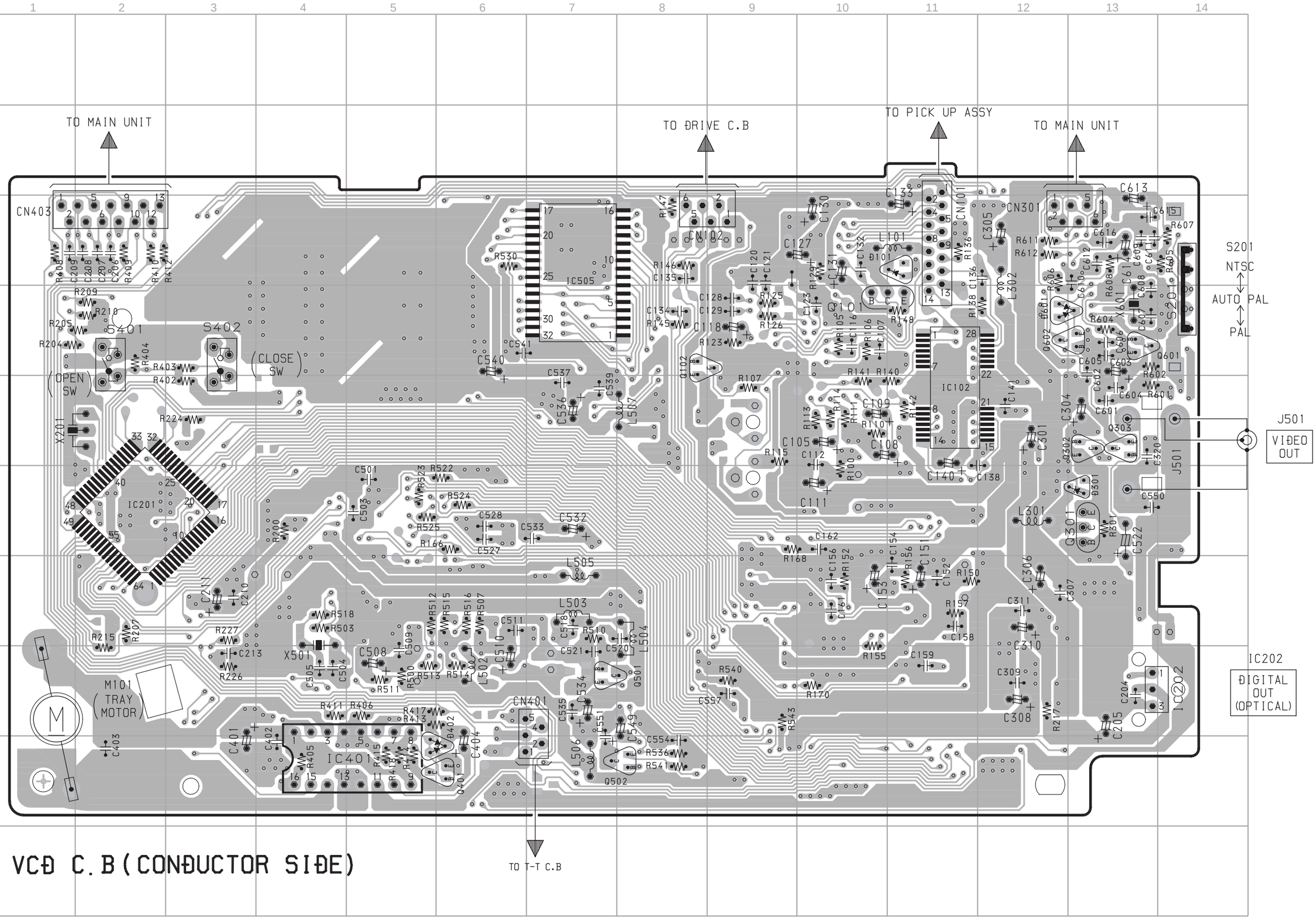
BLOCK DIAGRAM

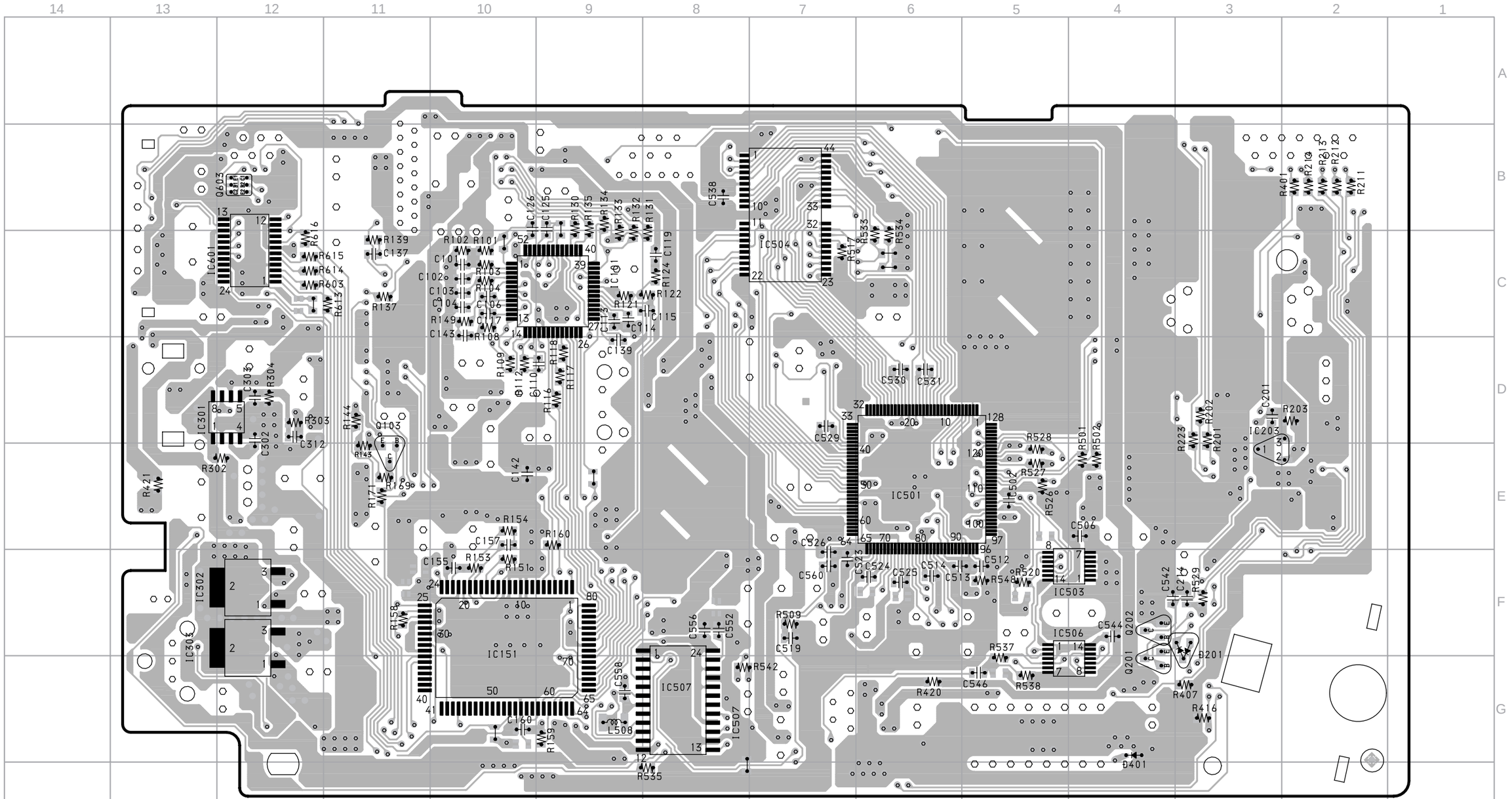


WIRING-1 (VOS1NDSHM, VOS1RNDSM, VOS1RNDSC)

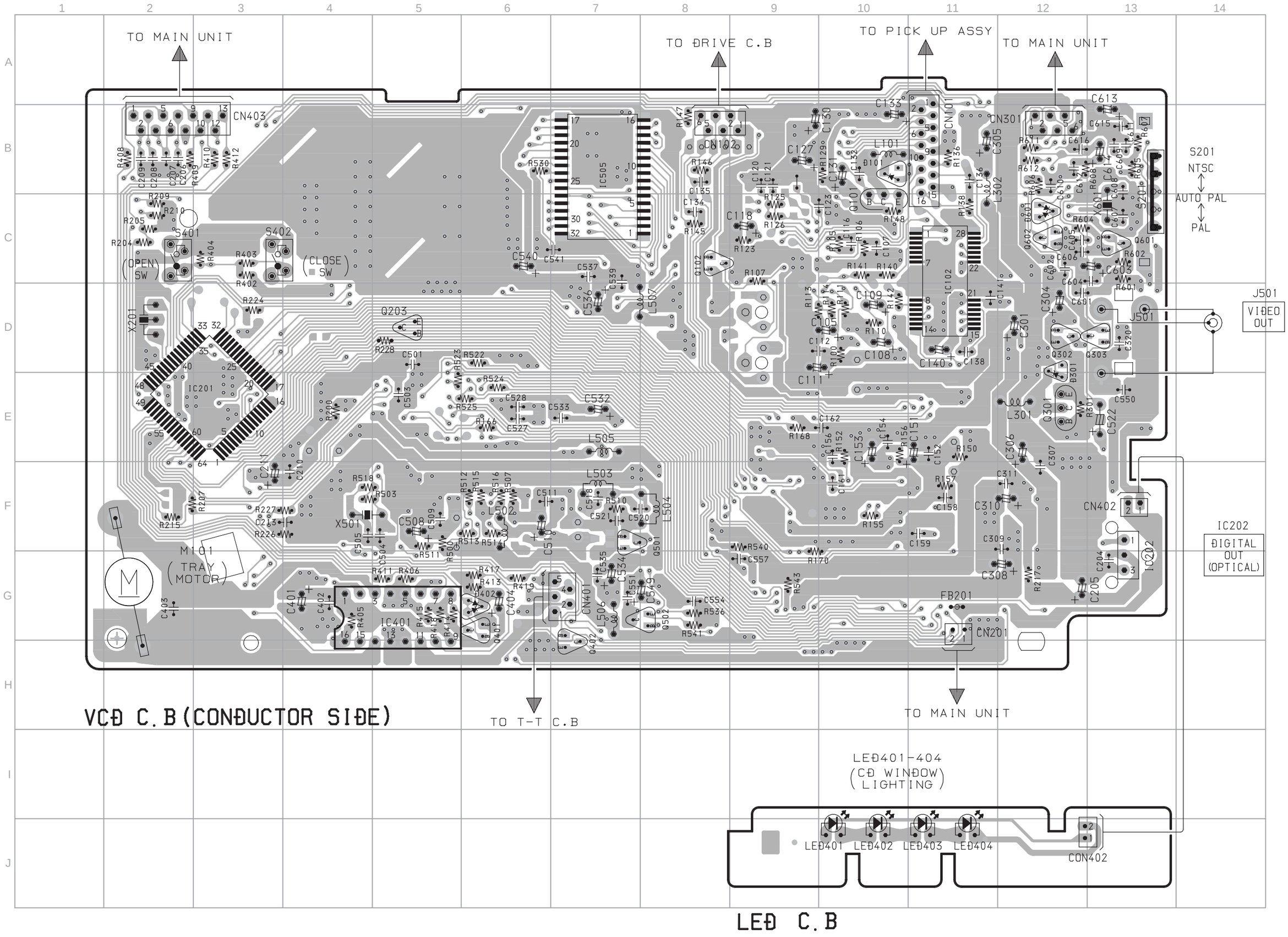


VCĐ C.B (CONĐUCTOR SIĐE)

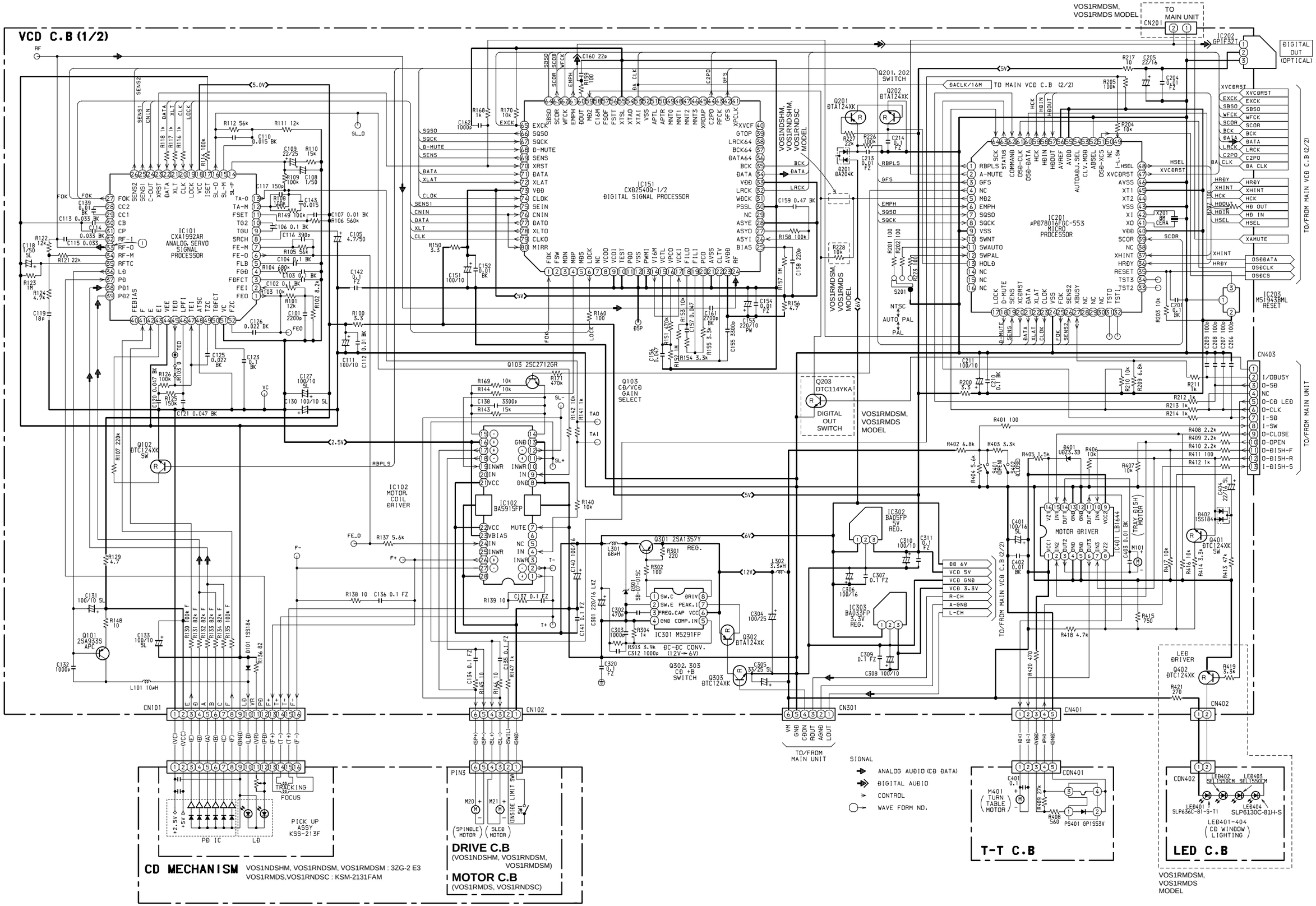


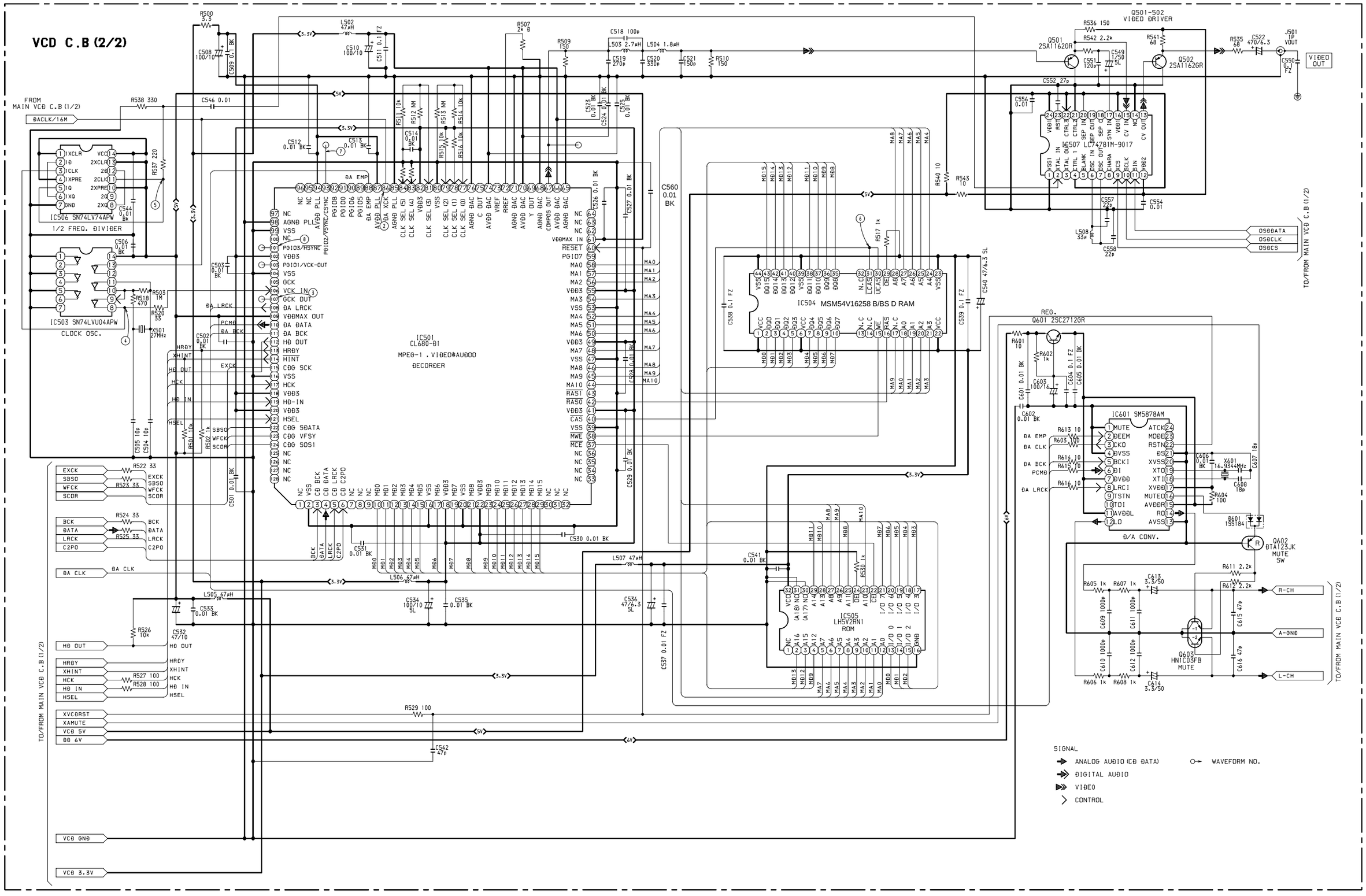


VCD C.B(COMPONENT SIDE)

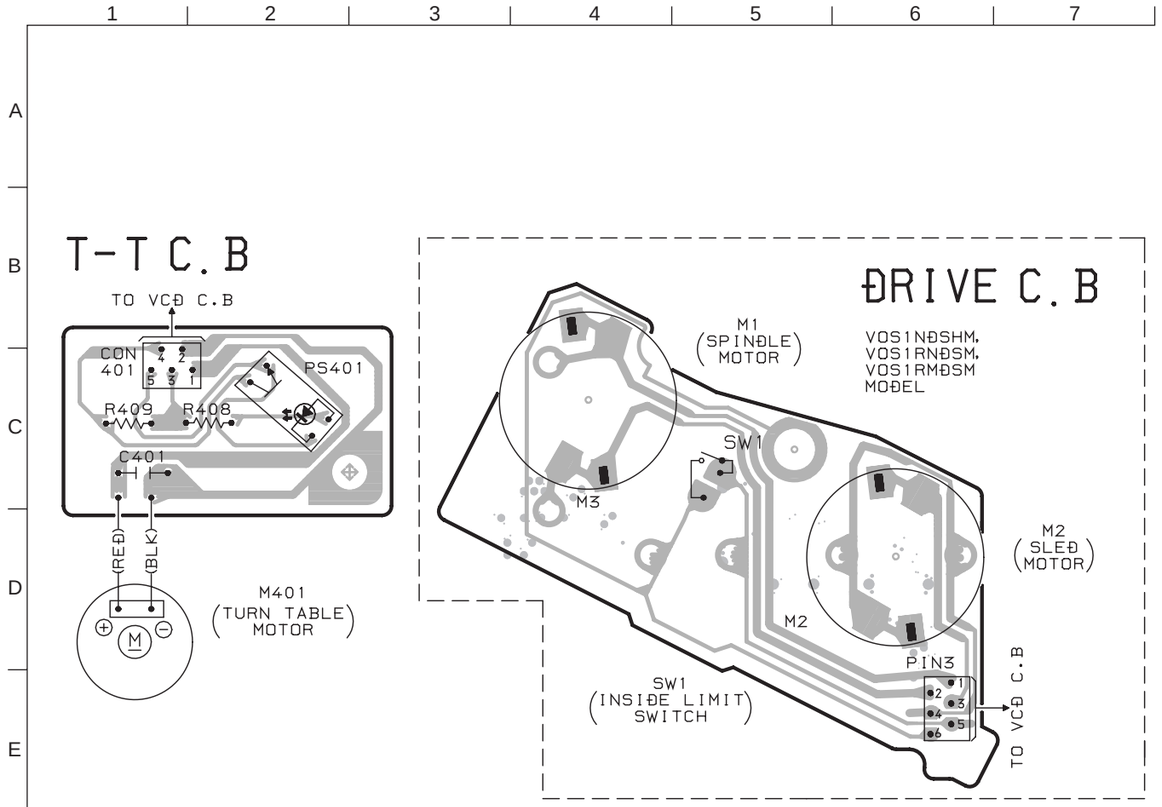

TO MAIN UNIT
TO ÐRIVE C.B
TO PICK UP ASSY
TO MAIN UNIT
CN403
CN102
CN1101
CN301
CN402
CN201
S401
S402
(OPEN) SW
(CLOSE) SW
M101 (TRAY MOTOR)
IC201
IC401
IC505
IC102
IC202
X201
X501
Q203
Q102
Q101
Q601
Q301
Q302
Q303
Q501
Q502
Q401
Q402
L101
L301
L302
L501
L502
L503
L504
L505
L506
L507
FB201
S201
NTSC
AUTO PAL
PAL
J501
VIÐEO OUT
IC202
ÐIGITAL OUT (OPTICAL)
VCÐ C.B(CONÐUCTOR SIÐE)
TO T-T C.B
TO MAIN UNIT
LEÐ401-404
(CÐ WINÐOW) LIGHTING
LEÐ401
LEÐ402
LEÐ403
LEÐ404
CON402
LEÐ C.B

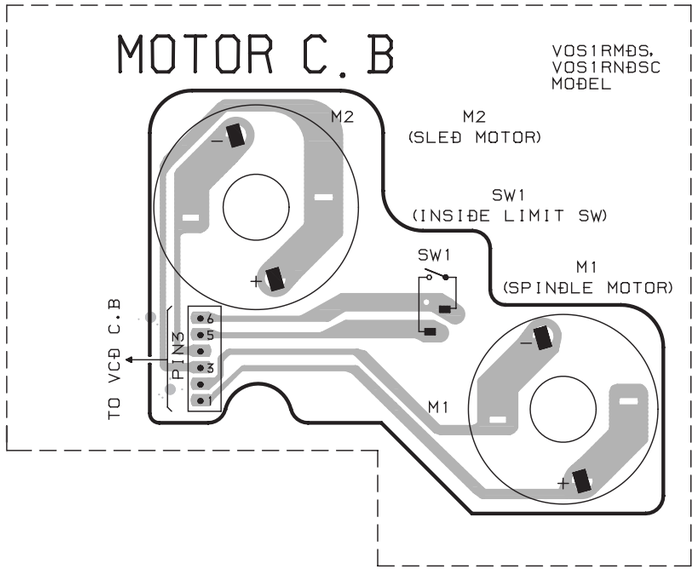
SCHEMATIC DIAGRAM-1




VCD C.B (2/2)
FROM MAIN VCD C.B (1/2)
BACLK/16M
1/2 FREQ. DIVIDER
IC506 SN74LV74APW
IC503 SN74LVU04APW
CLOCK OSC.
X501 27MHz
IC501 CL680-01
MPEG-1 . VIDEO&AUDIO DECORDER
IC504 MSM54V16258 B/BS D RAM
IC505 LH5V2RN1 ROM
LC507 LC74781M-9017
Q501-502 VIDEO DRIVER
Q501 2SA1162GR
Q502 2SA1162GR
VIDEO OUT
REG.
Q601 2SC2712GR
IC601 SM5878AM
D/A CONV.
Q602 DTA123JK MUTE SW
Q603 HN1C03FB MUTE
D601 1SS184
X601 16.9344MHz
R-CH
L-CH
A-GND
OSDDATA
OSDCLK
OSDCS
TO/FROM MAIN VCD C.B (1/2)
SIGNAL
ANALOG AUDIO (CD DATA)
DIGITAL AUDIO
VIDEO
CONTROL
WAVEFORM NO.

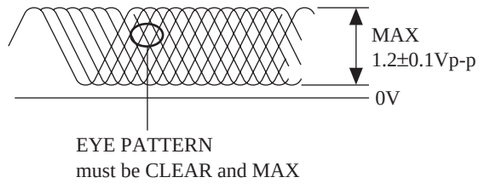
WIRING-3 (MECHA)





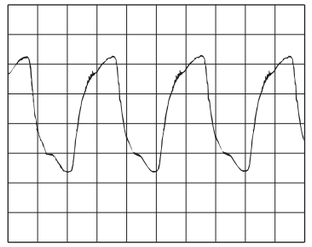
WAVE FORM

① IC101 Pin ㉝ (RF-O) VOLT/DIV: 200mV TIME/DIV: 0.5µS

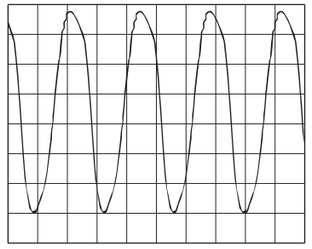


EYE PATTERN
must be CLEAR and MAX

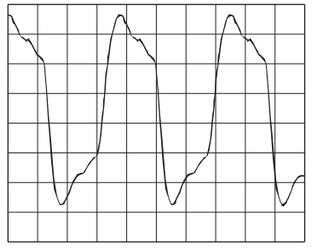
② IC501 Pin ㊱ DA XCK VOLT/DIV: 1V
16.93MHz TIME/DIV: 20nS



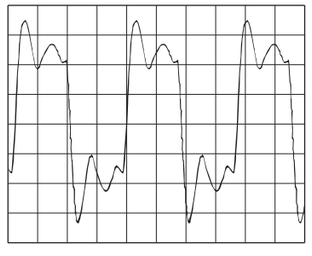
③ IC501 Pin ㊼ GCK OUT VOLT/DIV: 1V
42.3MHz TIME/DIV: 10nS



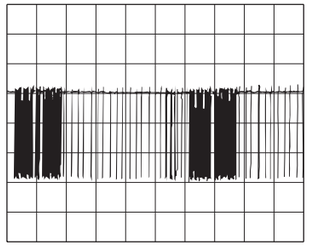
④ IC503 Pin ⑧ VCK VOLT/DIV: 1V
27MHz±1.35kHz TIME/DIV: 10nS



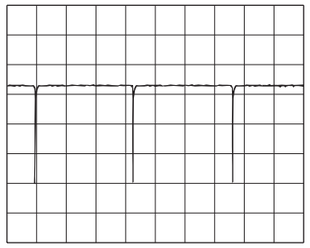
⑤ IC506 Pin ⑪ OSD CLK VOLT/DIV: 1V
13.5MHz±675Hz TIME/DIV: 20nS



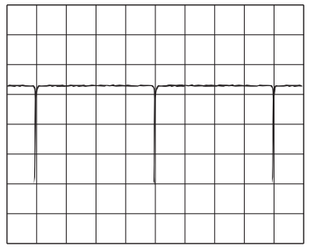
⑥ IC504 Pin ㉚ $\overline{UCAS}$ VOLT/DIV: 1V
(Pin ㉛ $\overline{LCAS}$) TIME/DIV: 2µS



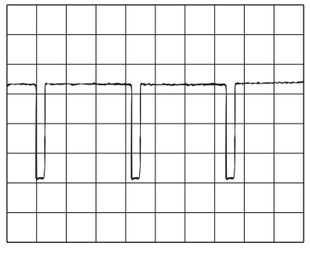
⑦ IC501 Pin ㉝ $\overline{VSync}$ VOLT/DIV: 1V
NTSC TIME/DIV: 5mS



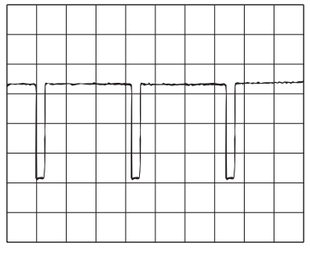
IC501 Pin ㉝ $\overline{VSync}$ VOLT/DIV: 1V
PAL TIME/DIV: 5mS



⑧ IC501 Pin ㉑ $\overline{HSync}$ VOLT/DIV: 1V
PAL TIME/DIV: 20µS



IC501 Pin ㉑ $\overline{HSync}$ VOLT/DIV: 1V
NTSC TIME/DIV: 20µS



IC DESCRIPTION

IC, CXA1992AR

Pin No.	Pin Name	I/O	Description
1	FEO	O	Output terminal for focus error amplifier. Internally connected to window comparator input for bias condition.
2	FEI	I	Input terminal for focus error.
3	FDFCT	I	Capacitor connection terminal for time constant used when there is defect.
4	FGD	I	This pin is connected to GND via capacitor when high frequency gain of the focus servo is attenuated.
5	FLB	I	This is a pin where the time constant is externally connected to raise the low frequency gain of the focus servo.
6	FE_O	O	Focus drive output.
7	FEM	I	Focus amplifier inverted input pin.
8	SRCH	I	This is a pin where the time constant is externally connected to generate the focus search waveform.
9	TGU	I	This is a pin where the selection time constant is externally connected to set the tracking servo the high frequency gain.
10	TG2	I	This is a pin where the selection time constant is externally connected to set the tracking high frequency gain.
11	FSET	I	Pin for setting peak of the phase compensator of the focus tracking.
12	TA_M	I	Tracking amplifier inverted input pin.
13	TA_O	O	Tracking drive output.
14	SL_P	I	Sled amplifier non-inverted input pin.
15	SL_M	I	Sled amplifier inverted input pin.
16	SL_O	O	Sled drive output.
17	ISET	I	The current which determines height of the focus search, track jump and sled kick is input with external resistance connected.
18	Vcc	I	Power supply.
19	LOCK	I	“L” setting starts sled disorder-prevention circuit. (Not pull-up resistance)
20	CLK	I	Clock input for serial data transfer from CPU. (No pull-up resistance)
21	XLT	I	Latch input from CPU. (No pull-up resistance)
22	DATA	I	Serial data input from CPU. (No pull-up resistance)
23	XRST	I	Reset system at “L” setting. (No pull-up resistance)
24	C_OUT	O	Signal output for track number counting.
25	SENS1	O	FZC, DFCT1, TZC, BALH, TGH, FOH, or ATSC is output depending on the command from CPU.
26	SENS2	O	DFCT2, MIRR, BALL, TGL or FOL is output depending on the command from CPU.
27	FOK	O	Output terminal for focus OK comparator.
28	CC2	I	Input pin where the DEFECT bottom hold output is capacitance coupled.
29	CC1	O	DEFECT bottom-hold output terminal. Internally connected to interruption comparator input.
30	CB	I	Connection terminal for DEFECT bottom-hold capacitor.
31	CP	I	Connection terminal for MIRR hold-capacitor. Anti-reverse input terminal for MIRR comparator.

Pin No.	Pin Name	I/O	Description
32	RF_I	I	Input terminal by capacity combination of RF summing amplifier.
33	RF_O	O	Output terminal of RF summing amplifier. Checkpoint of Eye pattern.
34	RF_M	I	Anti-reverse input terminal for RF summing amplifier. The gain of RF amplifier is decided by the connection resistance between RF_M and RFO terminals.
35	RFTC	I	This is a pin where the selection time constant is externally connected to control the RF level.
36	LD	O	APC amplifier output terminal.
37	PD	I	APC amplifier input terminal.
38, 39	PD1, PD2	I	RFI-V amplifier inverted input pin. These pins are connected to the A+C and B+C pins of the optical pickup, receiving by currents input.
40	FEBIAS	I/O	Bias adjustment pin of the focus error amplifier.
41, 42	F, E	I	F and EIV amplifier inverted input pins. These pins are connected to the F and E of the optical pickup, receiving by current input.
43	EI	—	Gain adjustment pin of the I-V amplifier E. (When not in use of BAL automatic adjustment)
44	VEE	—	GND connection pin.
45	TEO	O	Output terminal for tacking-error amplifier. Output E-F signal.
46	LPFI	I	BAL adjustment comparator input pin. (Input through LPF from TEO)
47	TEI	I	Input terminal for tracking error.
48	ATSC	I	Window-comparator input terminal for detecting ATSC.
49	TZC	I	Input terminal for tracking-zero cross comparator.
50	TDFCT	I	Capacitor connection pin for the time constant used when there is defect.
51	VC	O	Output terminal for DC voltage reduced to half of VCC+VEE.
52	FZC	I	Input terminal for focus-zero cross comparator.

IC, CXD2540Q

Pin No.	Pin Name	I/O	Description
1	FOK	I	Focus OK input. Used for SENS output and the servo auto sequencer.
2	FSW	O	Spindle motor output filter switching output.
3	MON	O	Spindle motor on/off control output.
4	MDP	O	Spindle motor servo control.
5	MDS	O	
6	LOCK	O	High, when sampled value of GFS at 460Hz is high. Low, when sampled value of GFS at 460Hz is low by 8 times successively.
7	NC	—	Not used.
8	VCOO	O	Analog EFM PLL oscillation circuit output.
9	VCOI	I	Analog EFM PLL oscillation circuit input. fLOCK=8.6436MHz.
10	TEST	I	TEST pin.
11	PDO	O	Analog EFM PLL charge pump output.
12	VSS	—	GND.
13	PWMI	I	Spindle motor external control input.
14	V16M	O	VCO2 oscillation output for the wide-band EFM PLL.
15	VCTL	I	VCO2 control voltage input for the wide-band EFM PLL.
16	VPCO	O	Wide-band EFM PLL charge pump output.
17	VCKI	I	VCO2 oscillation input for the wide-band EFM PLL.
18	FILO	O	Multiplier PLL (slave=digital PLL) filter output.
19	FILI	I	Multiplier PLL filter input.
20	PCO	O	Multiplier PLL charge pump output.
21	AVSS	—	Analog GND.
22	CLTV	I	Multiplier VCO1 control voltage input.
23	AVDD	—	Analog power supply (5V).
24	RF	I	EFM signal input.
25	BIAS	I	Constant current input of the asymmetry circuit.
26	ASYI	I	Asymmetry comparator voltage input.
27	ASYO	O	EFM full-swing output.
28	ASYE	I	Low: asymmetry circuit off; high: asymmetry circuit on.
29	NC	—	Not used.
30	PSSL	I	Audio data output mode switching input. Low: serial output; high: parallel output.
31	WDCK	O	D/A interface for 48-bit slot. Word clock f=2Fs.
32	LRCK	O	D/A interface for 48-bit slot. LR clock f=Fs.
33	VDD	—	Power supply (5V).
34	DA16	O	DA16 (MSB) output when PSSL=1. 48-bit slot serial data (two’s complement, MSB first) when PSSL=0.
35	DA15	O	DA15 output when PSSL=1. 48-bit slot bit clock when PSSL=0.
36	DA14	O	DA14 output when PSSL=1. 64-bit slot serial data (two’s complement, LSB first) when PSSL=0.
37	DA13	O	DA13 output when PSSL=1. 64-bit slot bit clock when PSSL=0.
38	DA12	O	DA12 output when PSSL=1. 64-bit slot LR clock when PSSL=0.

Pin No.	Pin Name	I/O	Description
39	DA11	O	DA11 output when PSSL=1. GTOP output when PSSL=0.
40	DA10	O	DA10 output when PSSL=1. XUGF output when PSSL=0.
41	DA09	O	DA09 output when PSSL=1. XPLCK output when PSSL=0.
42	DA08	O	DA08 output when PSSL=1. GFS output when PSSL=0.
43	DA07	O	DA07 output when PSSL=1. RFCK output when PSSL=0.
44	DA06	O	DA06 output when PSSL=1. C2PO output when PSSL=0.
45	DA05	O	DA05 output when PSSL=1. XRAOF output when PSSL=0.
46	DA04	O	DA04 output when PSSL=1. MNT3 output when PSSL=0.
47	DA03	O	DA03 output when PSSL=1. MNT2 output when PSSL=0.
48	DA02	O	DA02 output when PSSL=1. MNT1 output when PSSL=0.
49	DA01	O	DA01 output when PSSL=1. MNT0 output when PSSL=0.
50	APTR	O	Aperture compensation control output. This pin outputs a high signal when the right channel is used.
51	APTL	O	Aperture compensation control output. This pin outputs a high signal when the left channel is used.
52	VSS	—	GND.
53	XTAI	I	Crystal oscillation circuit input.
54	XTAO	O	Crystal oscillation circuit output.
55	XTSL	I	Crystal selector input.
56	FSTT	O	2/3 frequency divider output for Pins 53 and 54.
57	FSOF	O	1/4 frequency divider output for Pins 53 and 54.
58	C16M	O	16.9344MHz output. (V16M output in CLV-W and CAV-W modes)
59	MD2	I	Digital-out on/off control. High: on; low: off
60	DOUT	O	Digital-out output.
61	EMPH	O	Outputs a high signal when the playback disc has emphasis, and a low signal when there is no emphasis.
62	WFCK	I	WFCK (write frame clock) output.
63	SCOR	O	Outputs a high signal when either subcode sync S0 or S1 is detected.
64	SBSO	O	Sub P to W serial output.
65	EXCK	I	SBSO readout clock input.
66	SQSO	O	Sub Q 80-bit and PCM peak, level metter and internal status outputs.
67	SQCK	I	SQSO readout clock input.
68	MUTE	I	High: mute; low: release
69	SENS	—	SENS output to CPU.
70	XRST	I	System reset. Reset when low.
71	DATA	O	Serial data input from CPU.
72	XLAT	O	Latch input from CPU. Serial data is latched at the falling edge.
73	VDD		Power supply (5V).
74	CLOK	O	Serial data transfer clock input from CPU.
75	SEIN	I	SENS input from SSP.
76	CNIN	I	Track jump count signal input.

Pin No.	Pin Name	I/O	Description
77	DATO	O	Serial data output to SSP.
78	XLTO	O	Serial data latch output to SSP. Latched at the falling edge.
79	CLKO	O	Serial data transfer clock output to SSP.
80	MIRR	I	Mirror signal input. Used when the number of tracks is 128 or more for the 2N-track jump and M track move of the auto sequencer.

Notes)

- The 64-bit slot is an LSB first, two's complement output, and the 48-bit slot is an MSB first, two's complement output.
- GTOP is used to monitor the frame sync protection status. (High: sync protection window open.)
- XUGF is the negative pulse for the frame sync obtained from the EFM signal. It is the signal before sync protection.
- XPLCK is the inverse of the EFM PLL clock. The PLL is designed so that the falling edge and the EFM signal transition point coincide.
- GFS goes high when the frame sync and the insertion protection timing match.
- RFCK is derived from the crystal accuracy, and has a cycle of 136µ.
- C2PO represents the data error status.
- XRAOF is generated when the 32K RAM exceeds the ±28F jitter margin.

IC, CL680

Pin No.	Pin Name	I/O	Description
1	NC	—	No connection.
2	VSS	—	GND.
3	CD BCK	I	Bit clock input from CD DSP.
4	CD DATA	I	Data input from CD DSP.
5	CD LRCK	I	LRCK input from CD DSP.
6	CD C2PO	I	C2 pointer input from CD DSP.
7-9	NC	—	No connection.
10-15	MD0-MD5	I/O	DRAM/ROM interface. (DATA)
16	VSS	—	Ground.
17	MD6	I/O	DRAM/ROM interface. (DATA)
18	VDD3	—	Power supply 3.3V.
19	MD7	I/O	DRAM/ROM interface. (DATA)
20	VSS	—	Ground.
21	MD8	I/O	DRAM/ROM interface. (DATA)
22	VDD3	—	Power supply 3.3V.
23-29	MD9-MD15	I/O	DRAM/ROM interface. (DATA)
30-36	NC	—	No connection.
37	$\overline{\text{MCE}}$	—	ROM chip enable.
38	$\overline{\text{MWE}}$	O	DRAM write enable.
39	VSS	—	Ground.
40	$\overline{\text{CAS}}$	O	DRAM/ROM interface.
41	VDD3	—	Power supply 3.3V.
42	$\overline{\text{RASO}}$	O	DRAM/ROM interface.
43	$\overline{\text{RASI}}$	O	
44-46	MA10-MA8	O	DRAM/ROM interface. (Address)
47	VSS	—	Ground.
48	MA7	O	DRAM/ROM interface. (Address)
49	VDD3	—	Power supply 3.3V.
50-52	MA6-MA4	O	DRAM/ROM interface. (Address)
53	VSS	—	Ground.
54	MA3	O	DRAM/ROM interface. (Address)
55	VDD3	—	Power supply 3.3V.
56-58	MA2-MA0	O	DRAM/ROM interface. (Address)
59	PGIO7	I/O	Programmable I/O.
60	$\overline{\text{RESET}}$	I	Reset input.
61	VDD MAX IN	—	Power supply - VDDMAX. (5.0V)
62-64	NC	—	No connection.
65	AGND DAC	—	Analog ground.
66	A DAC	—	Analog power supply (DAC) : 3.3V.
67	COMP OUT	O	Composite out.
68	AGND DAC	—	Analog ground.

Pin No.	Pin Name	I/O	Description
69	Y OUT	O	Video signal “Y” OUT.
70	AVDD DAC	—	Analog power supply (DAC) 3.3V.
71	AGND DAC	—	Analog ground.
72	R REF	I	Reference resistor input.
73	V REF	I	Voltage reference input.
74	AVDD DAC	—	Analog power supply (DAC) : 3.3V.
75	C OUT	O	Video signal “C” out.
76	AGND DAC	—	Analog ground.
77-79	CLK SEL0-2	I	Clock selection input.
80	VSS	—	Ground.
81	CLK SEL3	I	Clock selection input.
82	VDD3	—	Power supply 3.3V.
83, 84	CLK SEL4, 5	I	Clock selection input.
85	AGND PLL	—	Analog ground.
86	DA XCK	I	DA XCK (16.933MHz) input.
87	AVDD PLL	—	Analog power supply 3.3V.
88	DA EMP	O	DAC-emphasis output.
89, 90	PGIO5, O6	I/O	Programmable I/O.
91	PGIO0	I/O	
92	PGIO8	I/O	
93	$\overline{\text{VSYNC}}$/$\overline{\text{CSYNC}}$	O	$\overline{\text{VSYNC}}$/$\overline{\text{CSYNC}}$ output.
94	AVDD PLL	—	Analog power supply (PLL) 3.3V.
95	VID_DAC_CK	O	Video DAC clock.
96	PROC_CK	O	Processor clock.
97	AUD_XCK	O	Audio XCK.
98	AGND PLL	—	Analog ground.
99	VSS	—	Ground.
100	NC	—	No connection.
101	$\overline{\text{HSYNC}}$	O	$\overline{\text{HSYNC}}$ output.
102	VDD3	—	Power supply 3.3V.
103	VCK OUT	O	VCK out.
104	VSS	—	Ground.
105	GCK	I	Global clock signal input. (42.3MHz)
106	VCK	I	Video clock signal input. (27.0MHz)
107	GCK OUT	O	Global clock signal output. (27.0MHz)
108	DA LRCK	O	DAC-LRCK output.
109	VDD MAX OUT	—	Power supply (VDD MAX) : 5.0V.
110	DA DATA	O	DAC-PCM data output.
111	DA BCK	O	DAC-BIT clock output.
112	HD OUT	O	Micon interface. (Data out)
113	HRDY	O	Micon interface. (Host ready)

Pin No.	Pin Name	I/O	Description
114	$\overline{\text{HINT}}$	O	Micon interface. (Host interrupt)
115	CDG SCK	I	CD-G serial clock input.
116	VSS	—	Ground.
117	HCK	I	Micon interface. (Host clock)
118	VDD3	—	Power supply 3.3V.
119	HD IN	I	Micon interface. (Host data in)
120	VDD3	—	Power supply 3.3V.
121	HSEL	I	Micon interface. (Host select in)
122	CDG DATA	I	CD-G data input.
123	CDG VFSY	I	CD-G VFSY input.
124	CDG SOSI	I	CD-G SOSI input.
125	DSP-XCK	O	DSP-XCK output.
126-128	NC	—	No connection.

IC, LC74781M

Pin No.	Pin Name	I/O	Description
1	VSS1	—	GND connection terminal. (Digital ground terminal).
2	Xtal IN	I	External X'tal and capacitor for internal sync generator, or the external clock are connected to this terminal. (2fsc or 4fsc).
3	Xtal OUT	O	
4	CTRL1	I	Either the external clock input mode or the X'tal generator mode is selected by this selector terminal. L: X'tal generator mode, H: External clock input.
5	BLANK	O	Blank signal (character and the green ORed signal) is output from this terminal. (MODE 0: composite sync signal is output at H.) When reset ($\overline{RST}$ terminal = L), the X'tal clock signal is output. (It is not output when reset by the reset command).
6	OSC IN	I	External coil and capacitor for the character output dot clock generator are connected to this terminal.
7	OSC OUT	O	
8	CHARA	O	The character signal is output from this terminal. (MOD 0: when H, the external sync signal identification signal is output from this terminal. This output signal tells whether the external sync signal is present or not. When external sync signal is present, H is output.) When reset ($\overline{RST}$ terminal = L), the dot clock signal (LC oscillator) is output. (It is not output when reset by the reset command).
9	$\overline{CS}$	I	Enable signal for the serial data input is input to this terminal. The serial data input is enabled at L. Pull-up resistor is built-in. (Hysteresis input).
10	SCLK	I	Clock of the serial data input is input to this terminal. Pull-up resistor is built-in. (Hysteresis input).
11	SIN	I	Serial data input terminal. Pull-up resistor is built-in. (Hysteresis input).
12	VDD2	—	Power supply for the composite video signal level adjustment. (Analog power supply).
13	CV OUT	O	Composite video signal output terminal.
14	NC	—	Connected to GND or not connected.
15	CV IN	I	Composite video signal input terminal.
16	VDD1	—	Power supply (+5V digital power supply).
17	SYN IN	I	Video signal for the internal sync separator circuit is input to this terminal. (When the internal sync separator circuit is not used, the horizontal sync signal or composite sync signal is input to this terminal).
18	SEP C	—	Internal sync separator circuit bias voltage monitoring terminal.
19	SEP OUT	O	The composite sync output signal of the internal sync separator circuit is output from this terminal. (H: MOD 1. H: during internal sync mode. L: during external sync mode.) (When internal sync separator circuit is not used, the SYN IN input signal is output from this terminal).
20	SEP IN	I	The output signal of the SEP OUT terminal is integrated so that the vertical sync signal is input to this terminal. An integrator circuit must be connected between the SEP OUT terminal and this terminal. When this terminal is not used, it must be connected to VDD1.
21	CTRL2	I	When selecting any of the NTSC or PAL or PAL-M or PAL-N system, the pin setting has priority. When L, the NTSC system is selected after resetting. Selection of either NTSC or PAL or PAL-M or PAL-N system by the command becomes effective. H: PAL-M system.

Pin No.	Pin Name	I/O	Description
22	CTRL3	I	Controls whether or not to input the $\overline{\text{VSYNC}}$ signal to the SEPIN input. L: to input the $\overline{\text{VSYNC}}$ signal. H: not to input the $\overline{\text{VSYNC}}$ signal.
23	$\overline{\text{RST}}$	I	System reset input terminal. Pull-up resistor is built-in. (Hysteresis input).
24	VDD1	—	Power supply. (+5V digital power supply).

IC, µPD78016FGC

Pin No.	Pin Name	I/O	Description
1	RBPLS	O	RADIAL BALANCE PLUS.
2	AMUTE	O	AUDIO ANALOG MUTE (H=MUTE ON).
3	GFS	I	GFS.
4	XVCDMD	I	AUDIO/VIDEO CD MODE (L=VCD=SPINDLE GAIN UP).
5	MD2	O	DOUT MUTE CONT.
6	EMPH	I	EMPHASIS.
7	SQSO	I	SQDATA FROM CD.
8	SQCK	O	SQCLK TO CD.
9	VSS	—	GND.
10	SWNT	I	SW TV OUT MODE (L=NTSC).
11	SWAUTO	I	SW TV OUT MODE (L=NTSC/PAL AUTO).
12	SWPAL	I	SW TV OUT MODE (L=PAL).
13	EMERG	I	POWER EMERGENCY STOP (L*3sec=STOP).
14	NC	—	Nou used.
15	LPCSEL	I	“LPC ON/OFF (H=ON, NORMAL)”.
16	NC	—	Nou used.
17	LOCK	O	GFS (FRAME SYNC) LOCK (NO USE=H).
18	DMUTE	O	DIGITAL DATA OUT MUTE.
19	SENS	I	DSP SENS1 FROM CD.
20	XCDRST	O	CD RESET.
21	DATA	O	DATA TO CD.
22	XLAT	O	XLT TO CD.
23	CLOK	O	CLK TO CD.
24	VSS	—	GND.
25	FOK	I	FOCUS OK.
26	SENS2	I	SSP SENS2 FROM CD.
27	XBUSY	I/O	READY/BUSY I/O TO HOST OD.
28	NC	—	Nou used.
29	NC	—	
30	NC	—	
31	TST0	I/O	CHECK LAND.
32	TST1	I/O	
33	TST2	I/O	
34	TST3	I/O	
35	RESET	I	RESET.
36	HRDY	I	HRDY FROM CL680.
37	XHINT	I	HINT FROM CL680.
38	NC	—	Nou used.
39	SCOR	I	SCOR FROM CD.
40	VDD	—	5.0VDD.
41	XO	O	8.0MHz CERALOCK.

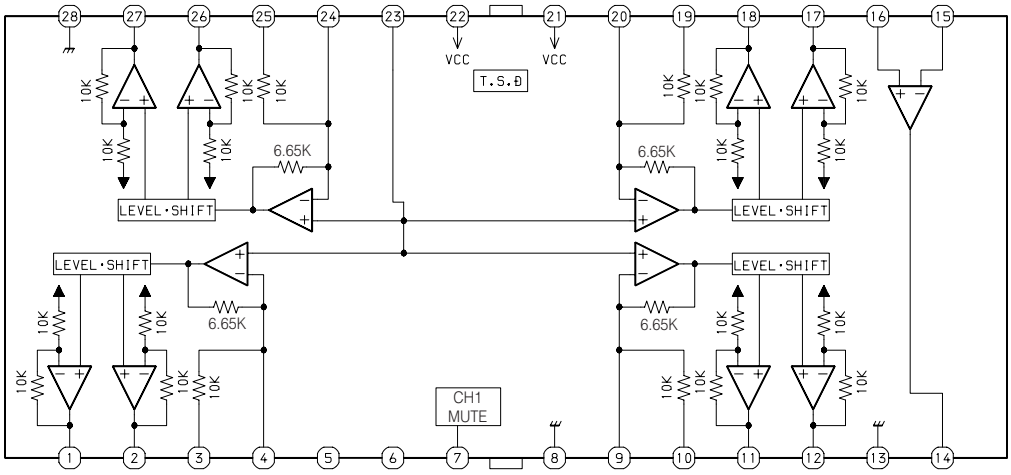
Pin No.	Pin Name	I/O	Description
42	XI	I	8.0MHz CERALOCK.
43	VSS	—	GND.
44	XT2	—	Nou used.
45	XT1	I	5.0VDD.
46	AVSS	—	GND.
47	XMPGRST	O	MPEG BLOCK IC RESET.
48	HSEL	O	ADDRESS/DATA SEL TO CL680.
49	INLSW	I	INSIDE LIMIT SW.
50	NC	—	Nou used.
51	OSDXCS	O	OSD CHIP SELECT.
52	ABSEL	I	CXA1992A/B SELECT (L=CXA1992A).
53	CLVSEL	I	CLV MODE SELECT (H=CLV-N).
54	AADSEL	I	AUTO ADJUST SELECT (H=AUTO ON).
55	AVDD	—	5.0VDD.
56	AVREF	—	
57	HDOUT	I	HD-OUT FROM CL680.
58	HDIN	O	HD-IN TO CL680.
59	HCK	O	HCK TO CL680.
60	OSDDATA	O	OSD DATA.
61	OSDCLK	O	OSD CLOCK.
62	COMMAND	I	COMMAND FROM HOST.
63	STATUS	O	STATUS TO HOST.
64	SCK	I	SCK FROM HOST.

IC, SM5878M

Pin No.	Pin Name	I/O	Description
1	MUTE	I	MODE = H: Soft mute ON/OFF terminal. (Mute at H). MODE = L: Attenuator level DOWN/UP terminal. (DOWN at H).
2	DEEM	I	De-emphasis ON/OFF terminal. (De-emphasis ON at H).
3	CKO	O	Oscillator clock output. (16.9344 MHz).
4	DVSS	—	Digital VSS terminal.
5	BCKI	I	Bit clock input terminal.
6	DI	I	Serial data input terminal.
7	DVDD	—	Digital VDD terminal.
8	LRCI	I	Sample rate clock (fs) input terminal. (H = L ch/L = R ch).
9	TSTN	I	Test input. (“H” or open during normal operation)
10	TO1	O	Test output 1. (Normally low level output).
11	AVDDL	—	Analog VDD terminal. (For L ch).
12	LO	O	Left channel analog output terminal.
13	AVSS	—	Analog VSS terminal.
14	RO	O	Right channel analog output terminal.
15	AVDDR	—	Analog VDD terminal. (For R ch).
16	MUTEO	O	Infinity zero detection output.
17	XVDD	—	X’tal system VDD terminal.
18	XTI	I	X’tal oscillator terminal. (Or external clock input terminal of 16.9344 MHz).
19	XTO	O	X’tal oscillator terminal.
20	XVSS	—	X’tal system VSS terminal.
21	DS	I	Double-speed/normal playback selection. (Double-speed at H).
22	RSTN	I	Reset terminal. (Reset at L).
23	MODE	I	Soft mute/Attenuator mode selection. (Soft mute at H).
24	ATCK	I	Attenuator level setup clock (Ignored when MODE = H).

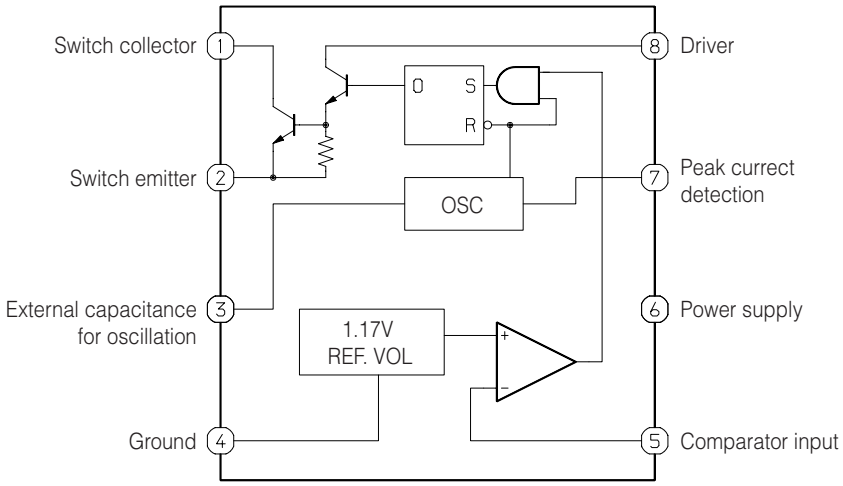
IC BLOCK DIAGRAM

IC, BA5915FP

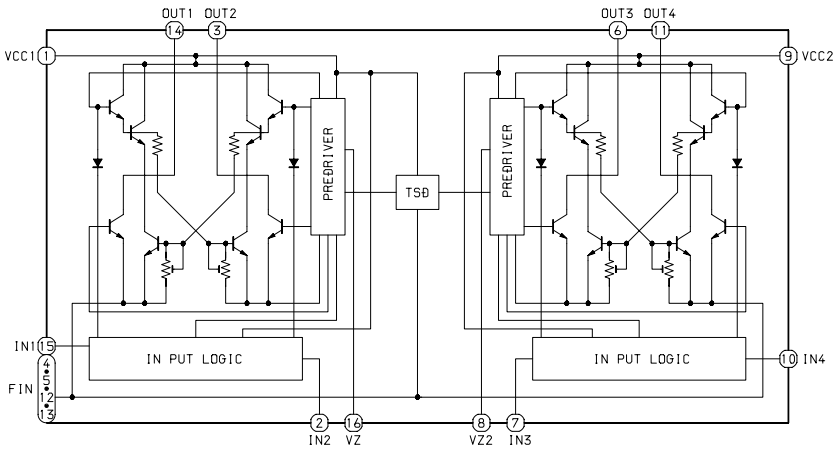


T.S.D: Thermal shut-down
Resistors are in units of Ω.

IC, M5291FP



IC, LB1644



TRUH TABLE

IN1	IN2	OUT1	OUT2	IN3	IN4	OUT3	OUT4
0	0	L	L	0	0	L	L
1	0	H	L	1	0	H	L
0	1	L	H	0	1	L	H
1	1	L	L	1	1	L	L

INPUT			OUTPUT				MODE	
IN1	IN2.3	IN4	OUT1	OUT2	OUT3	OUT4	M1	M2
0	0	0	L	L	L	L	BRAKE	BRAKE
1	0	0	H	L	L	L	FF/REW	BRAKE
0	1	1	L	H	L	L	REW/FF	BRAKE
1	1	0	L	L	H	L	BRAKE	FF/REW
0	0	1	L	L	L	H	BRAKE	REW/FF
1	1	1	L	L	L	L	BRAKE	BRAKE

TEST MODE

1. How to Activate CD Test Mode
   Insert the AC plug while pressing the function CD button.
   All FL display tubes will light up, and the test mode will be activated.

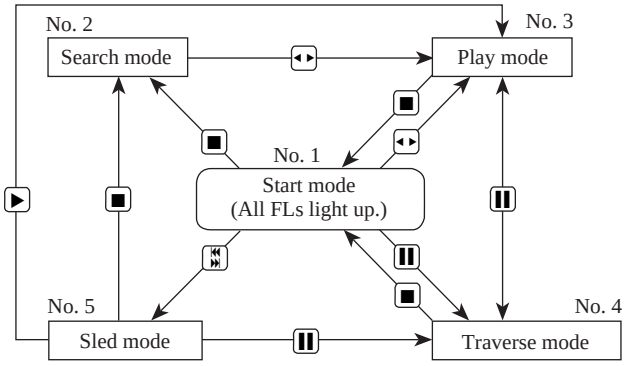
2. How to Cancel CD Test Mode
   Either one of the following operations will cancel the CD test mode.
   - Press the function button. (except CD function button)
   - Press the power switch button.
   - Disconnect the AC plug

3. CD Test Mode Functions
   When test mode is activated, the following mode functions from No.1 to No.5 can be used by pressing the operation keys.

Mode/No.	Operation	FL display	Operation	Contents
Start mode No.1	Activation	TEST 00 00 00 Flashes repeatdly	• Test mode is activated. • CD block power is ON.	• Test mode
Search mode No.2	■ key		• Continual focus search (The pickup lens repeats the full-swing up-down motion.) * Avoid continual searches that last for more than 10 minutes. * NOTE 1	FOCUS SERVO • Check focus search waveform • Check focus error waveform (FOK/FZC are not monitored in the search mode)
Play mode No.3	◀▶ key		• Normal playback • Focus search is continued if TOC cannot be read. * NOTE 1	FOCUS SERVO/TRACKING SERVO CLV SERVO/SLED SERVO Check FOK/FZC
Traverse mode No.4	▌▌ key		• During normal disc playback Press once; tracking servo OFF Press twice; tracking servo ON * NOTE 2	TRACKING SERVO ON/OFF Tracking balance (traverse) check
Sled mode No.5	⏮ key ⏭	All lamps light	• Pickup moves to the outermost track • Pickup moves to the innermost track * NOTE 3 (During playback, machine operates normally.)	SLED SERVO Check SLED mechanism operation

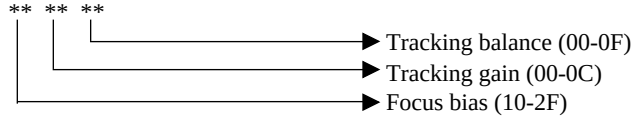
* NOTE 1: There are cases when the tracking servo cannot be locked owing to the protection circuit being operated when heat builds up in the driver IC if the focus search is operated continually for more than 10 minutes. In these cases the power supply should be switched off for 10 minutes until heat has been reduced and then re-started.
* NOTE 2: Do not press the ⏮ or ⏭ keys when the machine is in the ▌▌ status is active. If they are pressed, playback will not be possible after the ▌▌ status has been canceled. If the ⏮ or ⏭ keys are pressed in the ▌▌ status, press the ■ key and return to the start mode (No.1).
* NOTE 3: When pressing the ⏮ or ⏭ keys, take care to avoid damage to the gears. Because the sled motor is activated when the ⏮ or ⏭ keys are pressed, even when the pick-up is at the outermost or innermost track.

4. Operation Outline
   The operation of each mode is carried out in the direction of the arrows from the start mode as indicated in the following illustration.



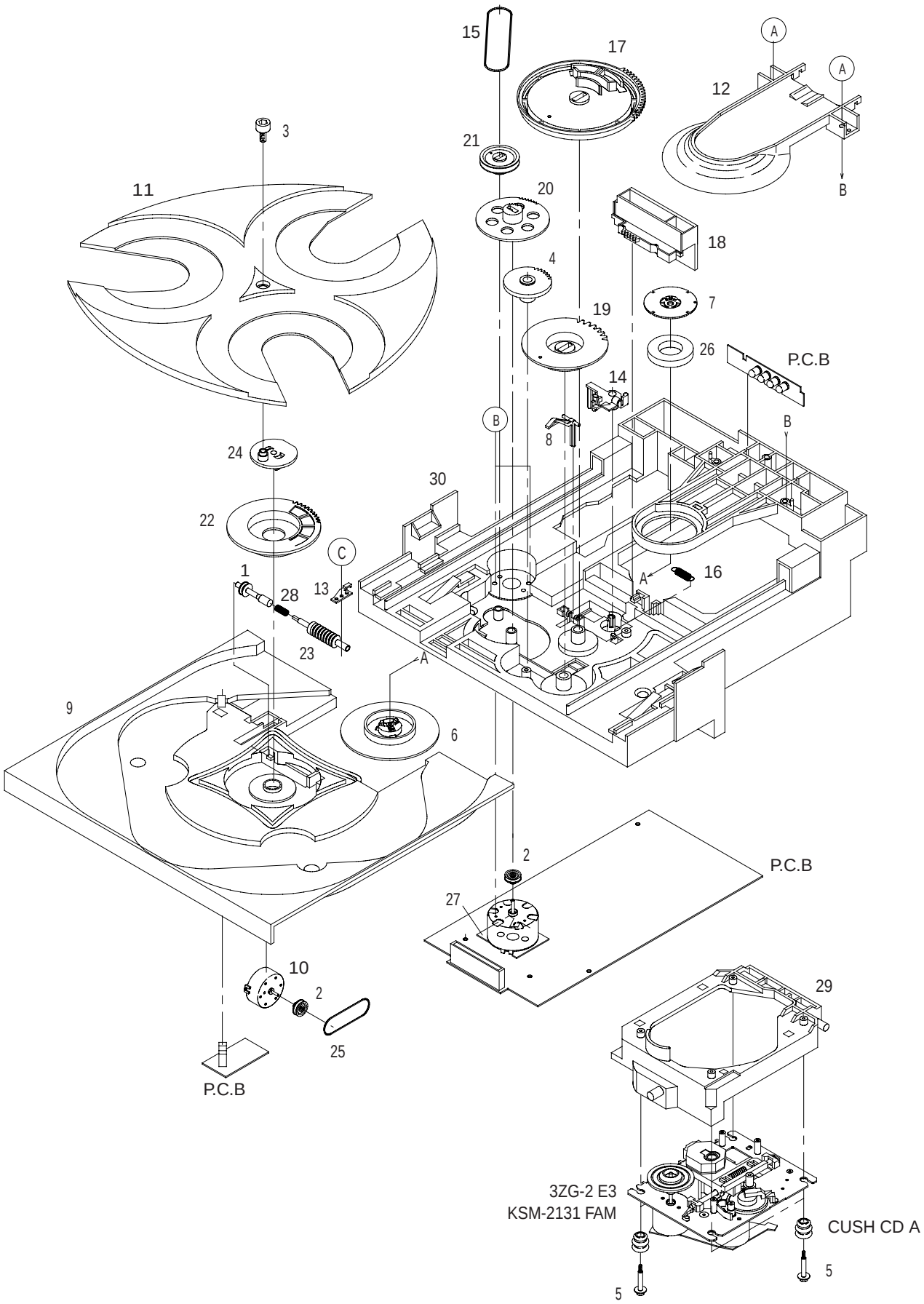
   If the DISC DIRECT PLAY button is pressed, the machine performs the same operation as the PLAY button is pressed as shown. If the tray is opened by pressing OPEN/CLOSE button during Play mode or Traverse mode, the machine returns to the Start mode.

5. How to check the Automatic Adjustment Values
   The automatic adjustment values can be checked by pressing the square (■) button.
   FL display (displayed in hexadecimal values)



   Note) The reference value is “20 08 08”.

MECHANICAL EXPLODED VIEW 1/1



MECHANICAL PARTS LIST 1/1

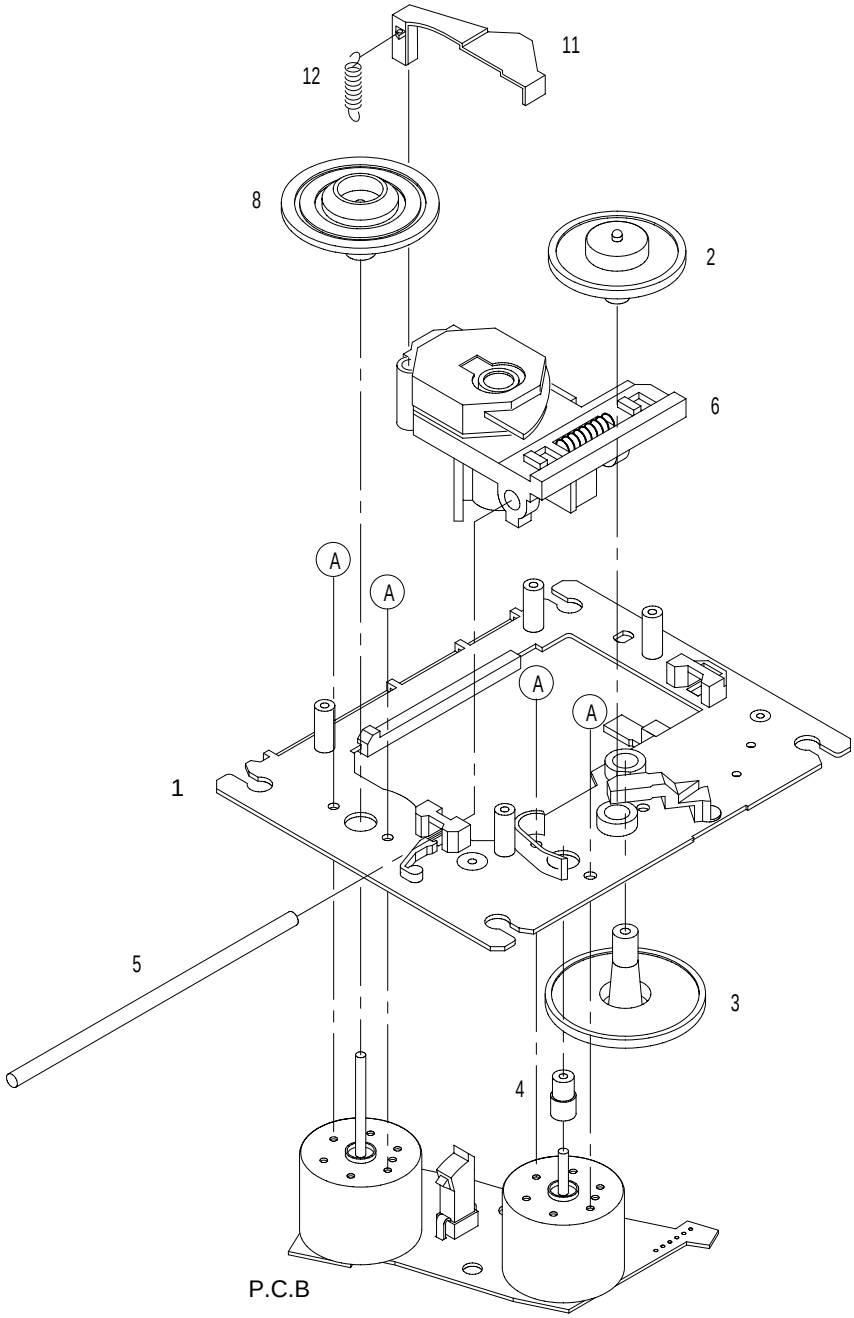
DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	84-ZG1-239-210		PULLY,WORM N<EXCEPT VOS1RNDSC>
1	84-ZG1-273-010		PULLEY,WORM 4<VOS1RNDSC>
2	84-ZG1-267-010		PULLEY,LOAD MO 8
3	81-ZG1-239-010		S-SCREW,TT
4	81-ZG1-291-110		GEAR,TRAY RELAY NO3
5	81-ZG1-271-010		S-SCREW MECH REAR
6	84-ZG1-289-010		HLDR,MAGNET NAT <VOS1NDSHM,VOS1RNDSM>
6	81-ZG1-277-310		HLDR,MAGNET N<VOS1RMDSM,VOS1RMDS>
6	84-ZG1-291-010		HLDR,MAGNET 4 NAT<VOS1RNDSC>
7	81-ZG1-255-110		PLATE,MAGNET MK2
8	83-ZG3-213-010		LVR,SW
9	84-ZG1-003-310		TRAY,NO2-B<VOS1NDSHM>
9	84-ZG1-008-210		TRAY,NO3<EXCEPT VOS1NDSHM>
10	87-045-364-010		MOTOR(BCH3B14)
11	84-ZG1-005-210		TURNTABLE,NO1(*)
12	84-ZG1-011-010		REFLECTOR,CD
13	84-ZG1-259-010		SPR-P,WORM
14	84-ZG1-266-010		LEVER,CAM 8<EXCEPT VOS1RNDSC>
14	84-ZG1-208-210		LEVER,CAM<VOS1RNDSC>
15	84-ZG1-209-010		BELT,SQ1.8-117.7
16	84-ZG1-211-010		SPR-E CAM S
17	84-ZG1-215-410		GEAR,MAIN CAM BLU <VOS1RMDSM,VOS1RMDS>
17	84-ZG1-203-410		GEAR,MAIN CAM <EXCEPT VOS1RMDSM,VOS1RMDS>
18	84-ZG1-216-310		SLIDE,MECHA CAM YEL <VOS1RMDSM,VOS1RMDS>
18	84-ZG1-204-310		SLIDER,MECHA CAM <EXCEPT VOS1RMDSM,VOS1RMDS>
19	84-ZG1-205-210		GEAR,TRAY (*)
20	84-ZG1-274-010		GEAR,RELAY 8<EXCEPT VOS1RNDSC>
20	84-ZG1-206-110		GEAR,RELAY<VOS1RNDSC>
21	84-ZG1-207-010		PULLEY,RELAY<EXCEPT VOS1RNDSC>
21	84-ZG1-271-010		PULLEY,RELAY 8<VOS1RNDSC>
22	84-ZG1-269-010		GEAR,MAIN TT 4
23	84-ZG1-238-010		GEAR,WORM N
24	84-ZG1-224-010		LEVER,TT<VOS1RMDSM,VOS1RMDS>
24	84-ZG1-288-010		LEVER,TT NAT <EXCEPT VOS1RMDSM,VOS1RMDS>
25	84-ZG1-225-010		BELT,SQ1.0-63.3
26	83-ZG3-604-010		RING,MAG 2
27	87-045-305-010		MOTOR, RF-500TB DC-5V (2MA) <EXCEPT VOS1RNDSC>
27	87-045-383-010		MOT,M9I50T28-2<VOS1RNDSC>
28	84-ZG1-248-010		SPR-C,WORM
29	84-ZG1-287-010		HLDR,MECHA NAT <EXCEPT VOS1RMDSM,VOS1RMDS>
29	84-ZG1-212-210		HLDR,MECHA NO2 <VOS1RMDSM,VOS1RMDS>
30	84-ZG1-286-010		CHAS,MECHA NAT <VOS1NDSHM,VOS1RNDSM>
30	84-ZG1-201-410		CHAS,MECHA<VOS1RMDSM,VOS1RMDS>
30	84-ZG1-292-010		CHAS,MECHA N NAT<VOS1RNDSC>
A	87-067-703-010		TAPPING SCREW, BVT2+3-10
B	87-251-070-410		U+2.6-3
C	87-067-981-010		BVT2+3-6 BLK

COLOR NAME TABLE

Basic color symbol	Color	Basic color symbol	Color	Basic color symbol	Color
B	Black	C	Cream	D	Orange
G	Green	H	Gray	L	Blue
LT	Transparent Blue	N	Gold	P	Pink
R	Red	S	Silver	ST	Titan Silver
T	Brown	V	Violet	W	White
WT	Transparent White	Y	Yellow	YT	Transparent Yellow
LM	Metallic Blue	LL	Light Blue	GT	Transparent Green
LD	Dark Blue	DT	Transparent Orange		

CD MECHANISM EXPLODED VIEW 1/1 (3ZG-2E3)

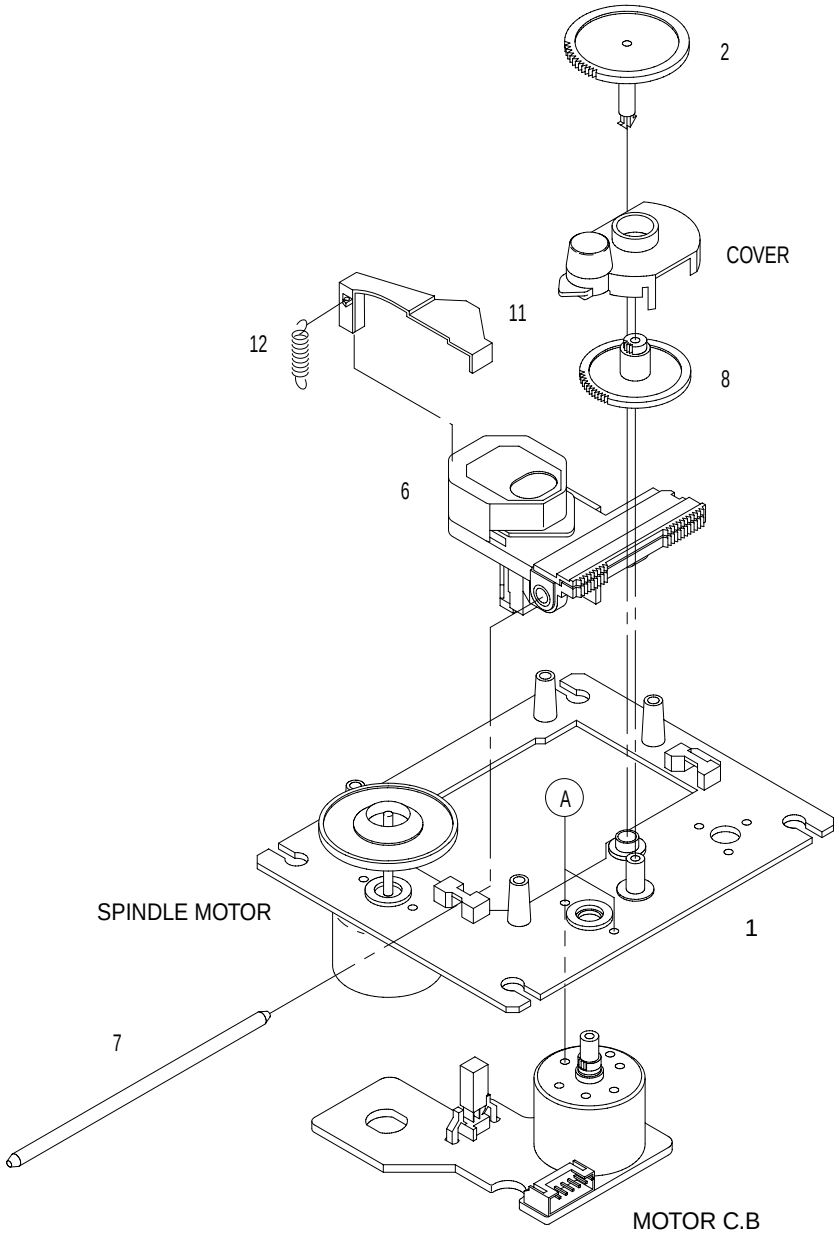


CD MECHANISM PARTS LIST 1/1 (3ZG-2E3)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	83-ZG2-243-210		CHAS ASSY,SHT
2	83-ZG2-235-010		GEAR,A3
3	83-ZG2-205-210		GEAR,B
4	83-ZG2-236-010		GEAR MOTOR 3
5	83-ZG2-253-010		SHAFT,SLIDE 5
6	87-A90-836-010		PICKUP,KSS-213F
8	83-ZG2-227-210		TURN TABLE,C1
11	83-ZG2-245-410		LEVER,SHUTTER
12	83-ZG2-250-110		SPR-E,SHT 2
A	87-261-032-210		SCREW V+2-3

CD MECHANISM EXPLODED VIEW 1/1 (KSM-2131 FAM)



CD MECHANISM PARTS LIST 1/1 (KSM-2131 FAM)

DESCRIPTIONで判断できない物は "REFERENCE NAME LIST" を参照してください。
If can't understand for Description please kindly refer to "REFERENCE NAME LIST".

REF. NO	PART NO.	KANRI NO.	DESCRIPTION
1	9X-262-629-220		MOTOR CHASSIS ASSY(MB)(FR)
2	92-626-907-010		GEAR(A)(S)
6	87-A90-836-010		OPTICAL PICK UP KSS-213F
7	92-626-908-020		SHAFT SLED
8	92-627-003-010		GEAR(B)
11	92-646-697-020		LENS SHUTTER(F)
12	92-646-702-010		SPRIG EXTENSION
A	97-621-255-150		SCREW+P2-3

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