# Full bridge current driven vertical deflection booster — TDA4865

## FEATURES

- Fully integrated, few external components
- No additional components in combination with the deflection controller TDA4850/51
- Pre-amplifier with differential high CMRR current mode inputs
- High electro-magnetic immunity
- Low offsets
- High linear sawtooth signal amplification
- High efficient DC-coupled vertical output bridge circuit
- Powerless vertical shift
- High deflection frequency up to 140 Hz
- Power supply and flyback supply voltage independent adjustable to optimize power consumption and flyback time
- Excellent transition behaviour during flyback
- Guard circuit for screen protection

## QUICK REFERENCE DATA

| SYMBOL | PARAMETER | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|
| **DC supply** | | | | | |
| $V_P$ | supply voltage range (pin 3) | 8 | – | 25 | V |
| $V_{FB}$ | flyback supply voltage (pin 7; note 2) | – | – | 60 | V |
| $I_{FB}$ | quiescent current (pin 7) | – | 12 | 18 | mA |
| **Vertical circuit** | | | | | |
| $I_{defl}$ | deflection current (peak-to-peak value; pins 4 and 6) | 0.6 | – | 2 | A |
| $I_{id}$ | differential input current (peak-to-peak value; note 3) | – | ±500 | ±600 | μA |
| **Flyback generator** | | | | | |
| $I_{FB}$ | maximum current during flyback (peak-to-peak value; pin 7) | – | – | ±1 | A |
| **Guard circuit** | | | | | |
| $V_8$ | guard voltage (guard on) | – | – | 12.5 | V |
| $I_8$ | guard current (guard on) | 5 | – | – | mA |

**Notes to the quick reference data**

1. Voltages refer to pin 5 (GND).
2. Up to 60 V ≥ $V_{FB}$ ≥ 40 V a decoupling capacitor $C_{FB}$ = 22 μF (between pin 7 and pin 5) and a resistor $R_{FB}$ = 100 Ω (between pin 7 and $V_{FB}$) are required (see Fig.4).
3. Differential input current $I_{id} = I_1 - I_2$.

## GENERAL DESCRIPTION

The TDA4865 is a power amplifier for use in 90 degree colour vertical deflection systems for frame frequencies of 50 Hz to 140 Hz. The circuit provides a high CMRR current driven differential input with high electro-magnetic immunity. Due to the bridge configuration of the two output stages DC-coupling of the deflection coil is achieved. In conjunction with TDA4850/51 the ICs offer an extremely advanced system solution.

## ORDERING INFORMATION

| EXTENDED TYPE NUMBER | PACKAGE | | | |
|---|---|---|---|---|
| | PINS | PIN POSITION | MATERIAL | CODE |
| TDA4865 | 9 | SIL | plastic | SOT110 |

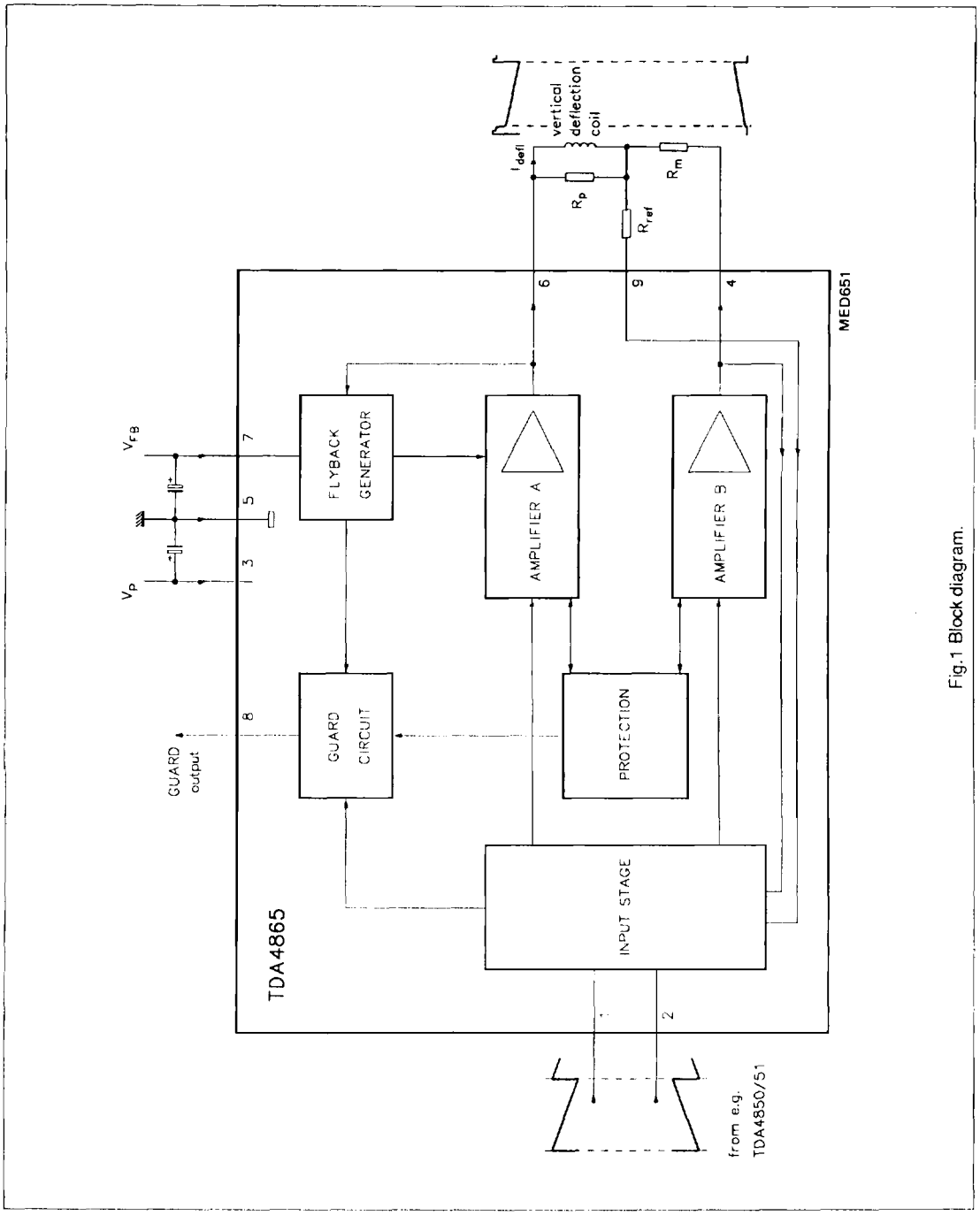


Fig.1 Block diagram.

## PINNING

| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| INA | 1 | input A |
| INB | 2 | input B |
| $V_P$ | 3 | supply voltage |
| OUTB | 4 | output B |
| GND | 5 | ground |
| OUTA | 6 | output A |
| $V_{FB}$ | 7 | flyback supply voltage |
| GUARD | 8 | guard output |
| FEEDB | 9 | feedback input |

The cooling fin is connected to pin 5 (GND)

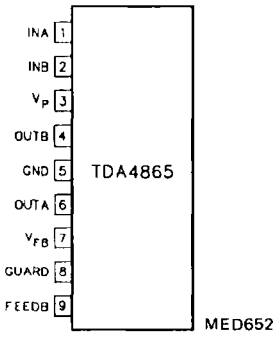


Fig.2 Pin configuration.

## FUNCTIONAL DESCRIPTION

The TDA4865 consists of a differential input stage, two output stages, a flyback generator, a protection circuit for the output stages and a guard circuit.

### Differential input stage

The differential input stage has a high CMRR differential current mode input (pins 1 and 2) that results in a high electro-magnetic immunity and is especially suitable for driver units with differential (e.g. TDA4850/51) and single ended current signals. Driver units with voltage outputs are simply applicable as well (e.g. two additional resistors are required). The differential input stage delivers the driver signals for the output stages.

### Output stages

The two output stages are current driven in opposite phase and work in combination with the deflection coil in a full bridge configuration. Therefore the TDA4865 needs no external coupling capacitor (e.g. 2200 µF) and works with one supply voltage $V_P$ and a separate adjustable flyback supply voltage $V_{FB}$. The deflection current through the coil ($I_{defl}$) is measured with the resistor $R_m$ which produces a voltage drop ($U_{rm}$) of:

$U_{rm}$ = (approx.) = $R_m \times I_{defl}$

At the feedback input (pin 9) a part of $I_{defl}$ is fed back to the input stage. The feedback input has a current input characteristic which holds the differential voltage between pin 9 and the output pin 4 on zero. Therefore the feedback current ($I_9$) through $R_{ref}$ is:

$$I_9 = \text{(approx.)} = \frac{R_m}{R_{ref}} \times I_{defl}$$

The input stage directly compares the driver currents into pin 1 and 2 with the feedback current $I_9$. Any difference of this comparison leads to a more or less driver current for the output stages. The relation between the deflection current and the differential input current ($I_{id}$) is:

$$I_{id} = I_9 = \text{(approx.)} = \frac{R_m}{R_{ref}} \times I_{defl}$$

Due to the feedback loop gain ($V_{U\,loop}$) and internal bondwire resistance ($R_{bo}$) correction factors are needed to determine the accurate value of $I_{defl}$:

$$I_{defl} = I_{id} \times \frac{R_{ref}}{R_m + R_{bo}} \times \left(1 - \frac{1}{V_{U\,loop}}\right)$$

with $R_{bo}$ = (approx.) ≈ 70 mΩ

and $\left(1 - \frac{1}{V_{U\,loop}}\right) = 0.98$

for $I_{defl}$ = 1 A

The deflection current can be adjusted from ±1 A to ±0.3 A by varying $R_{ref}$ when $R_m$ is fixed to 1 Ω. Because of its current mode the feedback input (pin 9) has high immunity against electro-magnetic interferences too. High bandwidth and excellent transition behaviour is achieved due to the transimpedance principle this circuit works with.

### Flyback generator

During flyback the flyback generator supplies the output stage A with the flyback voltage. This makes it possible to optimize power consumption (supply voltage $V_P$) and flyback time (flyback voltage $V_{FB}$). Due to the absence of a decoupling capacitor the flyback voltage is fully available.

### Protection

The output stages are fully protected against:

- Thermal overshoot
- Short circuit of the coil (pins 4 and 6)

### Guard circuit

The internal guard circuit gives information of any irregular values of the deflection current. The guard signal is active high:
- at thermal overshoot
- when feedback loop is out of range
- during flyback

The guard signal can be used to blank the CRT. The internal guard circuit will not be activated, if the input signals on pin 1 and 2 delivered from the driver circuit are out of range.
For this reason an external guard circuit can be applied to detect failures of the input signal too (see Fig.6; application proposal). This circuit will be activated when flyback pulses are missing, which is the indication of any abnormal operation.

## LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); voltages referring to pin 5 (GND) unless otherwise specified

| SYMBOL | PARAMETER | MIN. | MAX. | UNIT |
|---|---|---|---|---|
| $V_P$ | supply voltage (pin 3) | 0 | 30 | V |
| $V_{FB}$ | flyback supply voltage (pin 7) | 0 | 62 | V |
| $I_{FB}$ | flyback supply current | 0 | ±1.8 | A |
| $V_{1,2}$ | input voltage | 0 | $V_P$ | V |
| $I_{1,2}$ | input current | 0 | ±5 | mA |
| $V_{4,6}$ | output voltage | 0 | $V_P$ | V |
| $I_{4,6}$ | output current (note 1) | 0 | ±1.8 | A |
| $V_9$ | feedback voltage | 0 | $V_P$ | V |
| $I_9$ | feedback current | 0 | ±5 | mA |
| $V_8$ | guard voltage (note 2) | 0 | $V_P$ + 0.4 | V |
| $I_8$ | guard current | 0 | ±5 | mA |
| $T_{stg}$ | storage temperature range | −20 | +150 | °C |
| $T_{amb}$ | operating ambient temperature range | −20 | +75 | °C |
| $T_j$ | junction temperature (note 3) | −20 | +150 | °C |
| $V_{ESD}$ | electrostatic handling (note 4) | − | ±300 | V |

### Notes to the limiting values

1. Maximum output currents $I_4$ and $I_6$ are limited by current protection.
2. For $V_P$ > 13 V the guard voltage $V_8$ is limited to 13 V.
3. Internally limited by thermal protection; switching point > 150 °C.
4. Equivalent to discharging a 200 pF capacitor through a 0 Ω series resistor.

## THERMAL RESISTANCE

| SYMBOL | PARAMETER | THERMAL RESISTANCE |
|---|---|---|
| $R_{th\,j\text{-}c}$ | from junction to case | 8 K/W |

## CHARACTERISTICS

$T_{amb}$ = +25 °C; $V_P$ = 15 V; $V_{FB}$ = 40 V; voltages refer to pin 5 (GND) unless otherwise specified

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_P$ | supply voltage range (pin 3) | | 8 | – | 25 | V |
| $V_{FB}$ | flyback supply voltage (pin 7) | see note 1 | $V_P$ | – | 60 | V |
| $I_{FB}$ | quiescent current (pin 7) | no load; no signal | – | 12 | 18 | mA |
| **Input stage** | | | | | | |
| $I_{id}$ | differential input current ($I_{id} = I_1 - I_2$) (peak-to-peak value) | | – | ±500 | ±600 | µA |
| $I_{1,2}$ | single ended input current (peak-to-peak value) | see note 2 | 0 | ±300 | ±600 | µA |
| $D_i$ | common mode rejection ratio | see note 3 | – | –54 | – | dB |
| $V_1$ | input clamp voltage | $I_1$ = 300 µA | 2.7 | 3.0 | 3.3 | V |
| $V_2$ | input clamp voltage | $I_2$ = 300 µA | 2.7 | 3.0 | 3.3 | V |
| $TC_1$ | TC input clamp voltage on pin 1 | | 0 | – | ±800 | µV/K |
| $TC_2$ | TC input clamp voltage on pin 2 | | 0 | – | ±800 | µV/K |
| $V_{1-2}$ | differential input voltage | $I_{id}$ = 0 | 0 | – | ±10 | mV |
| $I_9$ | feedback current | | – | ±500 | ±600 | µA |
| $V_9$ | feedback voltage | | 1 | – | $V_P$ – 1.5 | V |
| $I_{idoff}$ | differential input offset current ($I_{idoff} = I_1 - I_2$) | $I_{defl}$ = 0; $R_{ref}$ = 1.5 kΩ; $R_m$ = 1 Ω | 0 | – | ±30 | µA |
| $TC_{off}$ | TC differential input offset shift | | 0 | – | ±50 | nA/K |
| $C_{INA}$ | input capacity pin 1 referring to GND | | – | – | 5 | pF |
| $C_{INB}$ | input capacity pin 2 referring to GND | | – | – | 5 | pF |
| **Output stages A and B** | | | | | | |
| $I_4$ | output current | | – | – | ±1 | A |
| $I_6$ | output current | | – | – | ±1 | A |
| $V_{6-5}$ | output A saturation voltage to GND | $I_6$ = 0.7 A | – | 1.5 | 1.8 | V |
| $V_{6-3}$ | output A saturation voltage to $V_P$ | $I_6$ = 0.7 A; see note 4 | – | 3 | 3.4 | V |
| $V_{4-5}$ | output B saturation voltage to GND | $I_4$ = 0.7 A | – | 1.5 | 1.8 | V |
| $V_{4-3}$ | output B saturation voltage to $V_P$ | $I_4$ = 0.7 A; see note 4 | – | 1.9 | 2.3 | V |
| Lin | linearity error | $I_{defl}$ = ±0.7 A; see note 5 | – | – | 2 | % |
| $V_4$ | DC output voltage | $I_{id}$ = 0 A; closed loop | 6.6 | 7.2 | 7.8 | V |
| $V_6$ | DC output voltage | $I_{id}$ = 0 A; closed loop | 6.6 | 7.2 | 7.8 | V |
| $G_{oi}$ | open loop current gain ($I_{4,6}/I_{id}$) | $I_{4,6}$ < 100 mA; see note 6 | – | 100 | – | dB |
| $G_{of}$ | open loop current gain ($I_{4,6}/I_9$) | $I_{4,6}$ < 100 mA; see note 6 | – | 100 | – | dB |
| $G_{if}$ | current ratio ($I_{id}/I_9$) | closed loop | – | –0.2 | – | dB |
| $I_{deflrip}$ | output ripple current versus supply ripple | $V_{Prip}$ = ±0.5 V; $I_{id}$ = 0; closed loop | – | ±1 | – | mA |

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| **Flyback generator** | | | | | | |
| $V_{7-6}$ | voltage drop during flyback<br>reverse<br>forward | <br>$I_{defl}$ = 0.7 A;<br>during flyback | <br>–<br>– | <br>–2<br>4 | <br>–3.0<br>5.2 | <br>V<br>V |
| $V_7$ | switching on threshold voltage | | $V_P - 1$ | – | $V_P - 0.2$ | V |
| $V_7$ | switching off threshold voltage | | $V_P - 2.6$ | – | $V_P - 0.9$ | V |
| $I_7$ | flyback current during flyback | | – | – | ±1 | A |
| **Guard circuit** | | | | | | |
| $V_8$ | output voltage | guard on | 7.7 | – | 12.5 | V |
| $V_8$ | output voltage | guard on; $V_P$ = 8 V | 6.9 | – | $V_P - 0.4$ | V |
| $I_8$ | output current | guard on | 5 | – | – | mA |
| $V_8$ | output voltage | guard off; $I_9$ = 0.3 mA | – | – | 0.4 | V |
| $I_8$ | output current | guard off; $V_9$ = 5 V | 0.5 | 1 | 1.5 | mA |
| $V_{8\,(ext.)}$ | allowable external voltage on pin 8 | see note 7 | 0 | – | $V_P + 0.3$ | V |

**Notes to the characteristics**

1. Up to 60 V ≥ $V_{FB}$ ≥ 40 V a decoupling capacitor $C_{FB}$ = 22 µF (between pin 7 and pin 5) and a resistor $R_{FB}$ = 100 Ω (between pin 7 and $V_{FB}$) are required (see Fig.4).
2. Saturation voltages of output stages A and B can be increased in case of negative input currents $-I_{1,2} > 500$ µA.
3. $D_i = \frac{I_{deflc}}{I_{idc}} \times \frac{I_{id}}{I_{defl}}$ with $I_{deflc}$ = common mode deflection current and $I_{idc}$ = common mode input current.
4. For $V_{FB} < (V_P + 7\ V)$ increasing of saturation voltages $V_{6-3}$ and $V_{4-3}$ is possible (reduced limiting level of the input stage).
5. Deviation of the output signal with respect to the input signal.
6. Frequency behaviour of $G_{oi}$ and $G_{ol}$:
   –3 dB open loop bandwidth (–45 °) at 15 kHz; second pole (–135 °) at 1.3 MHz;
   open loop gain at second pole (–135 °) 55 dB.
7. For $V_P < 12.6$ V is $V_{8\,(ext.)} = V_P + 0.3$ V.

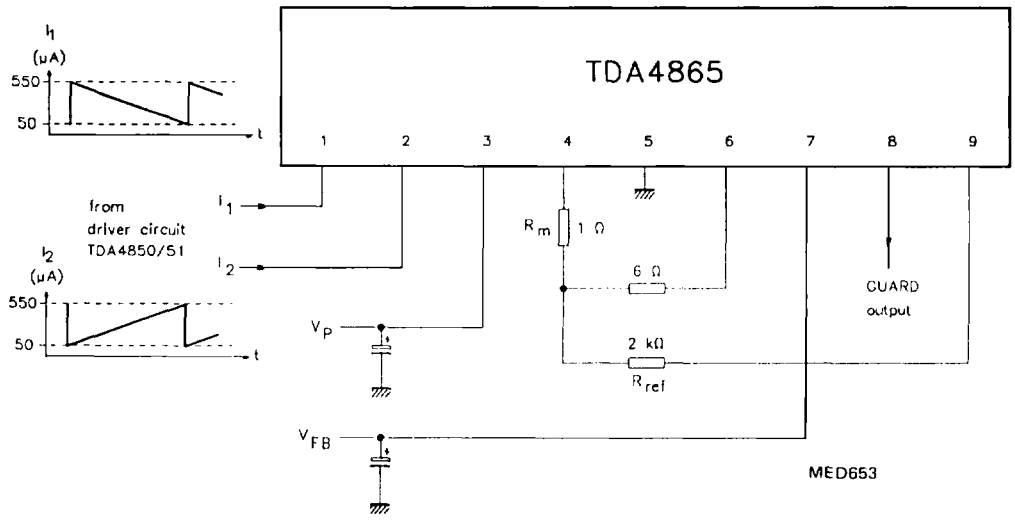


Fig.3 Test diagram.

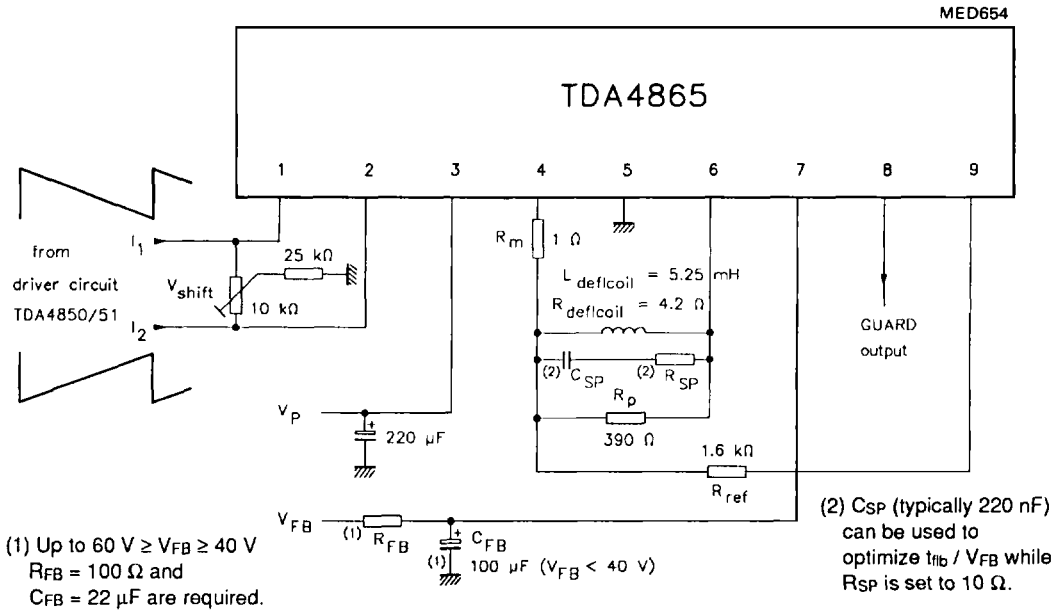


Fig.4 Application diagram with driver circuit TDA4850/51.

**Example**

Values given from application

| | | |
|---|---|---|
| $I_{deflmax}$ | = | 0.71 A |
| $L_{deflcoil}$ | = | 5.25 mH |
| $R_{deflcoil}$ | = | 4.17 Ω + 7% + ΔR(ϑ) |
| | = | 6.12 Ω |
| $R_m$ | = | 1 Ω + 1% |
| $R_p$ | = | 390 Ω |
| $R_{ref}$ | = | 1.6 kΩ |
| $V_{FB}$ | = | 40 V |
| $T_{amb}$ | = | +50 °C |
| $T_{jmax}$ | = | +110 °C |
| $T_{deflcoil}$ | = | +75 °C |

Calculated values

| | | |
|---|---|---|
| $V_P$ | = | 10 V |
| $t_{flb}$ | = | 250 µs |
| $P_{tot}$ | = | 4.5 W |
| $P_{defl}$ | = | 1.2 W |
| $P_{IC}$ | = | 3.3 W |
| $R_{thtot}$ | = | 60 K / 3.3 W ≈ 18 K/W |
| $R_{th\ j\text{-}c}$ | = | 8 K/W |

Therefore a heatsink with $R_{th\ c\text{-}a}$ < 10 K/W is needed.

Calculation formula for supply voltage and power consumption

$V_{b1} = V_{6-3} + R_{deflcoil} \times I_{deflmax} - U'_L + R_m \times I_{deflmax} + V_{4-5}$

$V_{b2} = V_{6-5} + R_{deflcoil} \times I_{deflmax} + U'_L + R_m \times I_{deflmax} + V_{4-3}$

for $V_{b1} > V_{b2}$ $V_P = V_{b1}$

for $V_{b2} > V_{b1}$ $V_P = V_{b2}$

with $U'_L = L_{deflcoil} \times 2\ I_{deflmax} \times f_v$

$f_v$ = vertical deflection frequency

$$P_{tot} = V_P \times \frac{I_{deflmax}}{\sqrt{3}} + V_P \times 0.003\ A + 0.05\ W + V_{FB} \times I_{FB}$$

$$P_{defl} = \frac{1}{3}\left(R_{deflcoil} + R_m\right) I^2_{deflmax}$$

$P_{IC} = P_{tot} - P_{defl}$

with $P_{IC}$ = power dissipation of the IC

$P_{defl}$ = power dissipation of the deflection coil

$P_{tot}$ = total power dissipation

Calculation formula for flyback time ($t_{flb}$)

$$t_{flb} \simeq \frac{L_{deflcoil}}{R_{deflcoil} + R_m} \ln\left(\frac{1 + \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} + V_{flbdr}}}{1 - \frac{(R_{deflcoil} + R_m) \times I_{deflmax}}{V_{FB} - V_{flbdf}}}\right) + t_{flboff}$$

with $t_{flboff}$ = flyback switch off time = 50 µs for this application ($t_{flboff}$ depends on $V_{FB}$, $I_{deflmax}$, $L_{deflcoil}$ and $C_{SP}$).

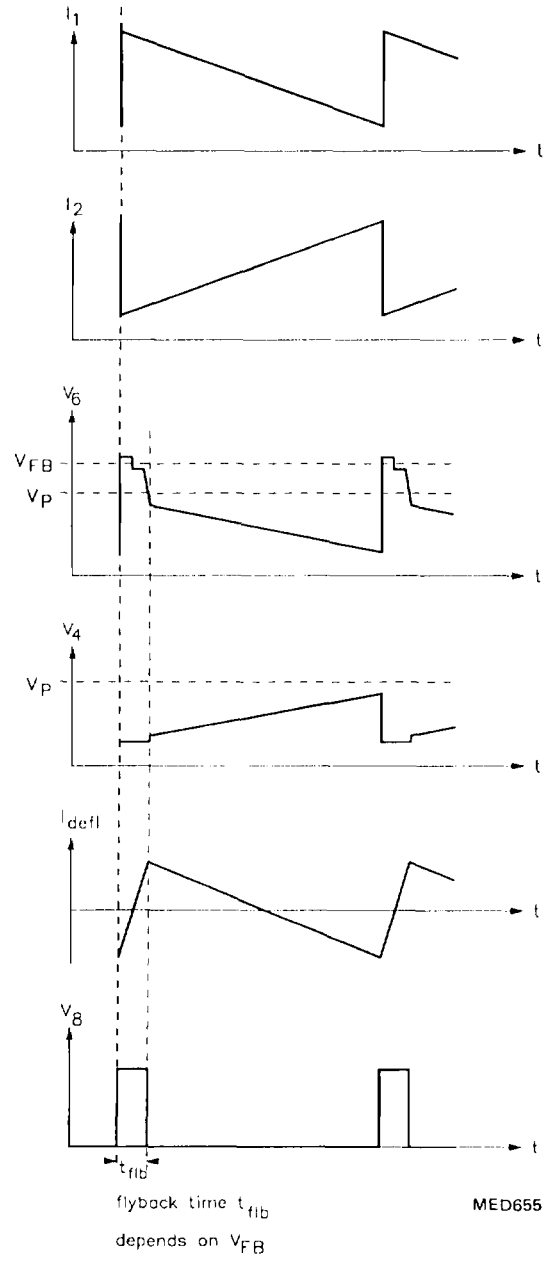


Fig.5 Timing diagram.

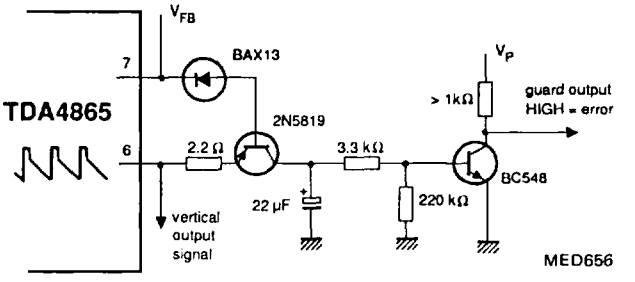


Fig.6 Application circuit for external guard signal generation.

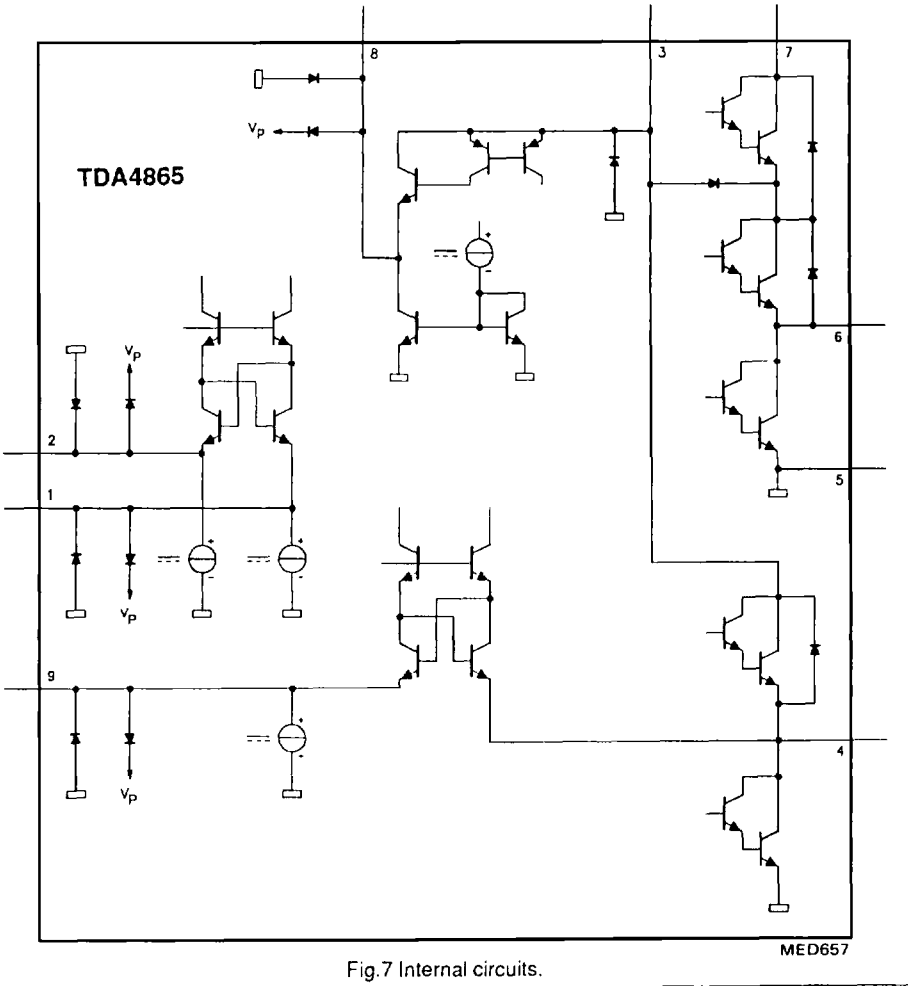


Fig.7 Internal circuits.