ROWA
乐华彩电

维 修 手 册

型号：LCD26P08/LCD26P08A
LCD32P08/LCD32P08A
LCD37P08/LCD40P08
LCD42P08/LCD42P08A

P08系列 中文维修手册仅用于维修参考

目录

1. 安全与注意事项

1.1 安全注意事项

(1) 为了持续保持安全，不要企图修改电路板。

(2) 在维修之前，断开交流电源。

(3) 维修技术人员配有任何时候都可以使用的准确电压表，这一点至关重要。定期检查电压表的校准。

(4) 请不要使显示器受强烈的外力震动。

1.2 操作使用注意点

(1) 移动显示器之前请拔掉电源接线。

(2) 为安全起见，一些部件被抬高，高过印刷电路板。有时，使用绝缘管或胶带。有时，内部接线被加起来，目的是为了防止与致热部件接触。把所有此类元件重新安装到其原来的位置

(3) 在维修后，要检查螺钉和接线是否正确地重新安装。要保证维修过的部件周围区域没有损坏。

(4) 请注意在长时间显示同一个画面后关机原来的图象信息可能还保持在上面。

(5) 检查交流插头的插片和易碰到的导电部件（如金属盘、输入端子和耳机塞孔）之间的绝缘情况。

1.3 高压警告

显示器高压是由电源升压板产生的，如果不注意接触到高压，可能被严重电击。

1.4 静电敏感器件（ESD）注意事项

一些半导体（固态）设备很容易被静电损坏，此类部件一般称为静电敏感器件器件（ESD）。典型的ESD器件有集成电路和一些场效应晶体管。下列方法会减少静电造成部件损坏时间的发生率。

1. 在处理任何半导体部件或组件之前，要立即通过接触已知的接地点，将静电从身体上放到。另一种发放是，带上放电的腕带装置。为了避免点击的危险，在给液晶电视加电之前，务必取下腕带。

2. 在拆除有ESD的组件后，将其放到导电平面（如铝箔）以防积聚静电。

3. 不要使用带氟利昂的化学品，这会产生足以破坏ESD的电荷。

4. 仅使用接地的铝铁焊接或焊开ESD.

5. 仅使用防静电除焊装置。一些不属于“防静电”类的除焊装置可能产生以破坏ESD的电荷。

6. 在准备安装之前，不要将设备用ESD由保护包装中取出。绝大多数用ESD包装有导线，这些导线通过导电泡沫与、铝箔或其它导电材料短接。

7. 即将由设备ESD导线上出去保护材料之前，应使保护材料与安装器件的地板和电路组件接触。

注意：不要给底板或电路加电并遵守其它安全注意事项。

8. 在处理没有包装的备用ESD时，要尽量减少身体的运动。一些运动如摩擦衣服或由铺地毯的地板上抬起脚都会产生足以破坏ESD的静电。

1.5 安装注意事项

1. 为了保障安全，搬运产品需要两人以上。

2. 让电源线远离散热设备，否则外壳融化可能导致起火或触电。

3. 不要将产品置于通风不良的区域，如书架和壁橱。内部温度升高可能造成起火。

4. 把外部天线接到产片上时，要弯曲内部天线。该措施旨在防止天线受潮。否则，可能造成起火或触电。

5. 必须保证在重新放置产品之前关闭电源并从插座拔下电源线。如果天线或外部链接器未完全插入，还应检查天线或外部连接器。天线损坏可能造成起火或触电。

6. 让天线远离高压线，并将天线安装牢靠。与高压线接触或天线掉下来可能造成起火或触电。

7. 当安装产品时，在产品和墙壁之间留下足够的空间（10cm），以便通风。

2. 液晶电视规格

2.1 基本规格

项目	液晶电视	
电视功能	电视标准	PAL B/G、D/K、I
	声音系统	FM-MONO
视频输入	视频1	RCA x 2(音频L/R x 2)
	视频2	RCA x 2(音频L/R x 2)
	S端子	x 1
	高清信号	Y、Pb、Pr x 1
	影音端子	HDMI x 1
PC 输入	信号输入	模拟:D-Sub 15 针
	即插即用兼容	DDC
	输入频率	模拟:FH:31.5kHz 到 50kHz FV:60Hz 到75Hz
	推荐	模拟:1360x768 (60Hz)
	音频输入	用于立体声的耳机迷你型插孔(3.5 ø)
视频输出功能	输出TV/AV1/AV2/	视频输出（RCA）
音频输出	音频输出音频输出:L/R	扬声器(内置)：6Wx2(L/R)
		用于立体声的耳机迷你型插孔(3.5 ø)
		声音输出(RCA L/R)
OSD 语言	中文/英文(出厂设定为中文)	
底座	可选	
墙壁装配件	可选	
电源	电源	AC 100V~240V, 50/60HZ
	功率消耗	26":120W/32":140W/37":200W/42":240W
使用环境	温度	+ 0 ° C ~ + 40 ° C
	储存温度	- 25 ° C ~ + 60 ° C
	湿度	10% ~ 85%
附件	遥控器、电池(AAAX2)、电源线、保修单、使用说明书	
电脑支持的格式	640 x 480 (60/75Hz)	
	800 x 600 (60/75Hz)	
	1024 x 768 (60Hz)	
	1360x768(60Hz)	
高清支持的模式	480i/p	
	576i/p	
	720p	
	1080i/p	

2.2 LCD TV 描述

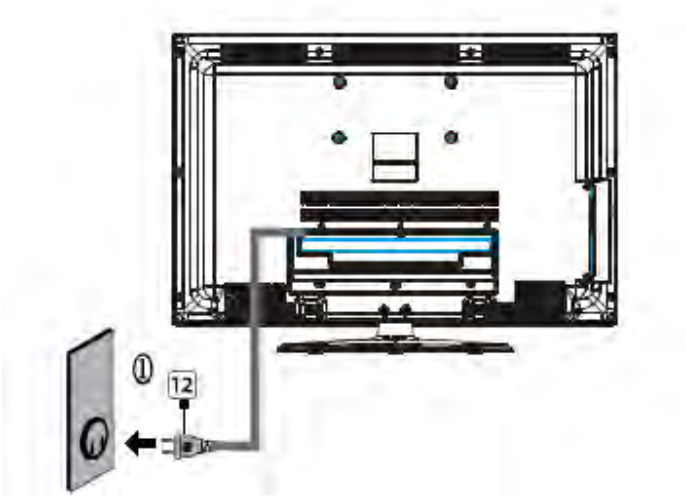
该 LCD TV 包含主板（内置音频板）、开关电源板（含逆变器）、遥控接收板、按键板。主板和电源板含 I_2C 逻辑控制总线，DDC，LCD panel 的亮度逻辑控制和通过DC-DC 转换器来提供整个主板和TTL信号给液晶模块去驱动LCD显示电路。

2.3 电源连接

将电源线一端插入本机后下方的“交流输入”插孔内，另一端接入市电220V的电源插座上。

在您未切断电源而处于待机的情况下，电视机始终会消耗部份功率。

在长时间不使用电视情况下 ， 最好将下面的电源开关关闭并将电源线从电源插座中拔下。



3 操作说明及调整

3.1 遥控器说明

电源
按这个键可以打开或待机，但电视不会完全断电，处于节能状态。

信源
按此键可显示当前可选信源，按▲、▼选择

0-9 0-9
用来选择电视频道。

显示
(1)当使用电视信号时显示频道号码及声音模式。
(2)当使用电视信号之外的其它输入时，显示当前输入源等信息

回看
用来显示前一次选择的电视频道。

音量+、-键
在进入菜单状态时可以用作确认和参数调整；在未进入菜单时为音量的加减。

频道+、-键 、
在进入菜单时进行上下选择在未进入菜单时

静音
中断声音或恢复声音。

菜单
菜单下是返回主菜单，在信源下是确认功能

图像大小
包含2 种模式,重复按可切换为满屏/标准。

方向键 、、、
在菜单中选择各个子菜单

声音模式
可选择关、立体声、新闻、电影、音乐、环绕音与自设定。

彩色模式
调整成标准色温，暖色温与冷色温

睡眠
使用这个按键，您可以设置电视在多长时间之后进入待机状态。重复按这个键可以在 关闭、15、30、45、60、90 和120 分钟之间选择。(定时器从菜单消失之后所选择的分钟开始倒数计时。

图像制式
可以快捷更改TV制式。

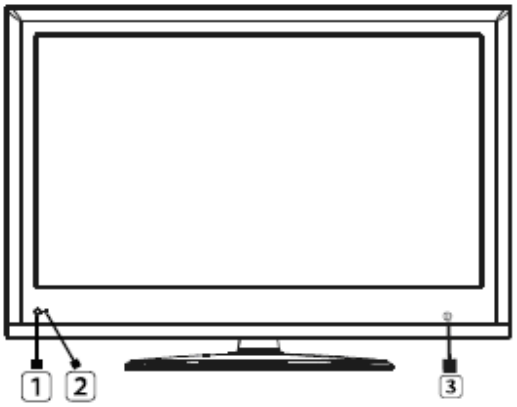
图像静止
打开与关闭画面静止

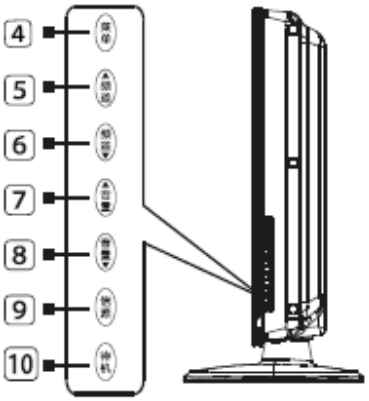
丽音
选择丽音通道

3.2 正面示意及控制面板

正面示意图

（具体结构请以实物为准）





按键示意图

❶ 遥控接收窗
❷ 指示灯
❸ 主电源开关
❹ 菜单键
❺ 节目增键
❻ 节目减键
❼ 音量增键
❽ 音量减键
❾ 信源键
❿ 待机键

待机键:	按此键可以打开或使电视进入待机状态，如果电视处在待机状态，则前面的指示灯会亮起红色。
信源键:	按此键可以变换不同的输入信源。
菜单:	按此键可以进入或退出菜单。
节目增减键:	在屏幕出现菜单时，按此两键可以选择所要执行选项，在屏幕无OSD 菜单时，为TV模式时可以换台。
音量增减键:	在屏幕出现菜单时，按此两键可以确认所选择之选项，在屏幕无OSD 菜单时，为音量之调整。

3.3 菜单功能

使用菜单
1. 按菜单按钮可以显示或关闭菜单菜单。
2. 使用左或右键可以选择所要调整之菜单选项。
3. 使用上或下键可以进入子菜单表，或启用或调整所选择之功能，光标所在位置为调整状态。
4. 按菜单按钮可以退出菜单。

电视/视频信源下的菜单画面
（注意：在不同的信源下，所能调节的功能有所不同）

按菜单按钮进入主菜单，调节项目包括：**图像、声音、系统、高级、电视、电脑**。请见以下详述：

图像

1. 图像模式-选择合适的图像效果（注：四种状态可选，分别是标准、艳丽、柔和、用户）。
2. 对比度-调节画面黑白层次，适当的对比度可使画面清晰明亮。
3. 亮度-调节画面的背景亮度，一般与对比度配合使用。
4. 色调-调节色彩的色调（注：只在NTSC制式图像状态下才可以选择和调整功能）。
5. 饱和度-调节色彩的鲜艳度、饱和度（注：电脑状态下无此选项）。
6. 清晰度-调节画面清晰度（注：电脑状态下无此选项）。
7. 色温-调节画面的冷暖感觉（注：三种状态可选，分别是标准、暖色、冷色）。
8. 图像大小-选择合适的图像模式（注：两种状态可选，分别是满屏和标准）。

声音

1. 声音模式-调节声音模式（注：四种状态可选，分别是用户、标准、新闻、音乐）。
2. 低音-调节电视机的声音低频效果。
3. 高音-调节电视机的声音高音效果。
4. 平衡-调节左右音箱大小比例、

系统

1. 菜单语言-选择语言的种类（注：两种语言可选，分别是中文、英文）。
2. 菜单透明度-选择调节OSD的透明亮度。
3. 复位-初始化设置。

高级

1. 图像降噪-图像噪点抑制（注：有四种状态可选，分别是关、低、中、高）
2. 睡眠时间-设定睡眠关机时间（注：有七种状态可选，分别是关、15、30、45、60、90、120）

电视

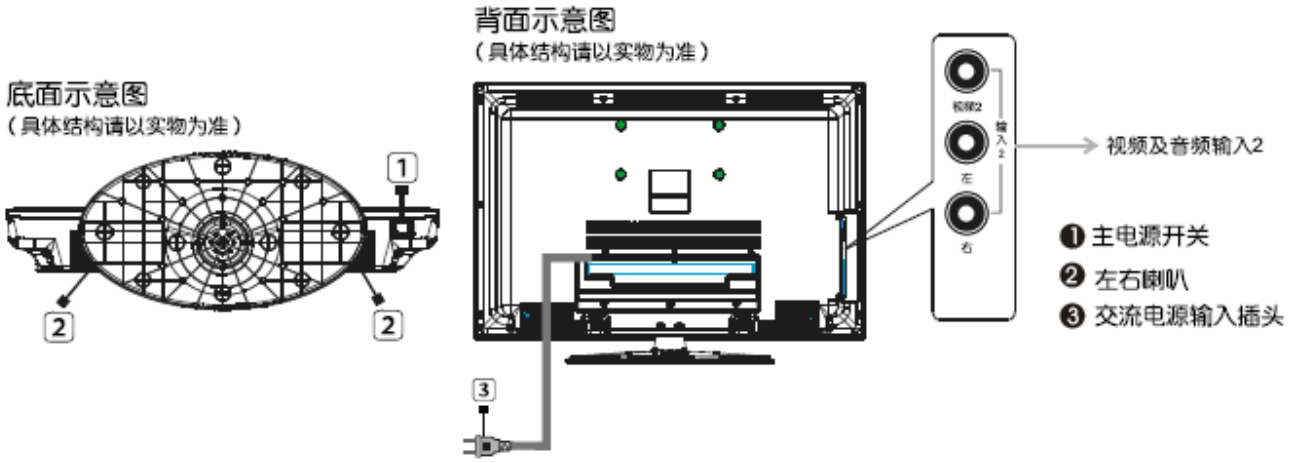
1. 频道-选择频道。
2. 彩色制式-选择视频信号制式（有三种状态可选，分别是自动、PAL、SECAM）。
3. 声音制式-选择伴音信号制式（有四种状态可选，分别是D/K、M、B/G、I）。
4. 跳跃-台号跳跃功能。
5. 微调-微调功能
6. 手动搜台-手动搜台功能。
7. 自动搜台-自动搜台功能。
8. 丽音-选择丽音或者单声道（注:当地电视台如有发送丽音伴音信号，才能选择。）

电脑(只在电脑信源下有作用)

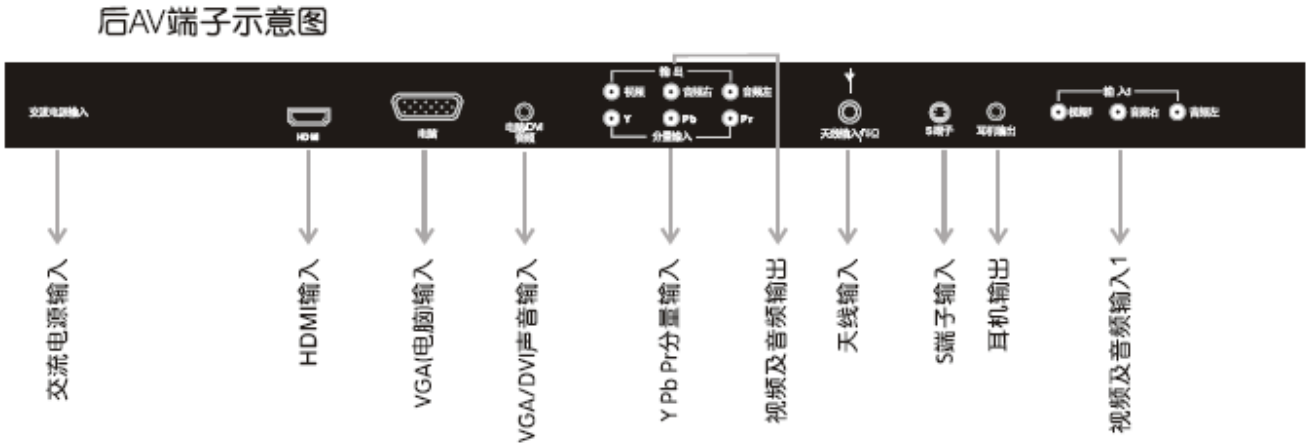
1. 水平位置-调节画面的水平位置。
2. 垂直位置-调节画面的垂直位置。
3. 时钟-调节画面的时钟频率。
4. 相位-调整A/D的采样相位。
5. 自动-自动调节屏幕显示到最佳状态

4.连接介绍

4.1 底面及背面连接示意图

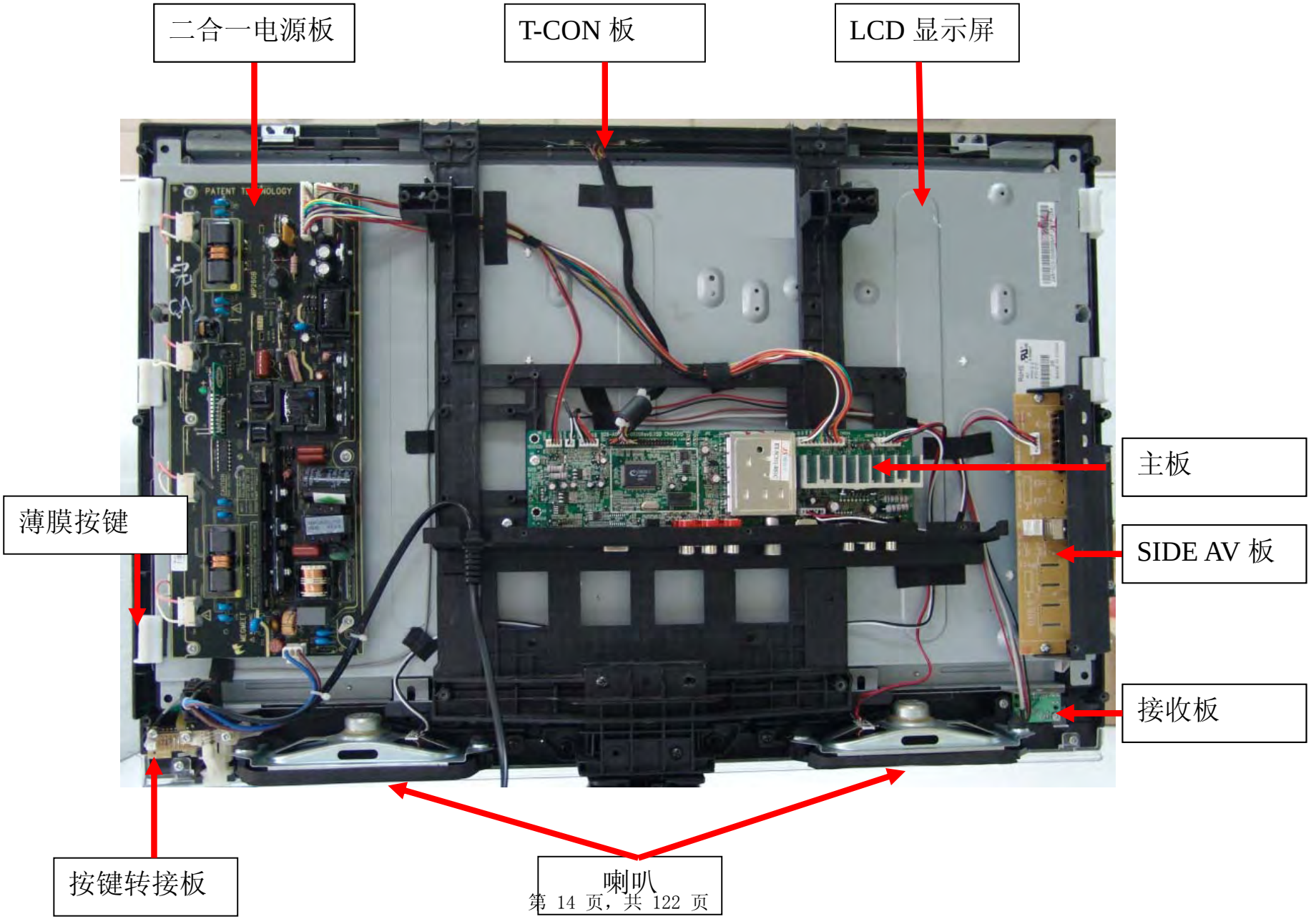


4.2 后AV端子示意图

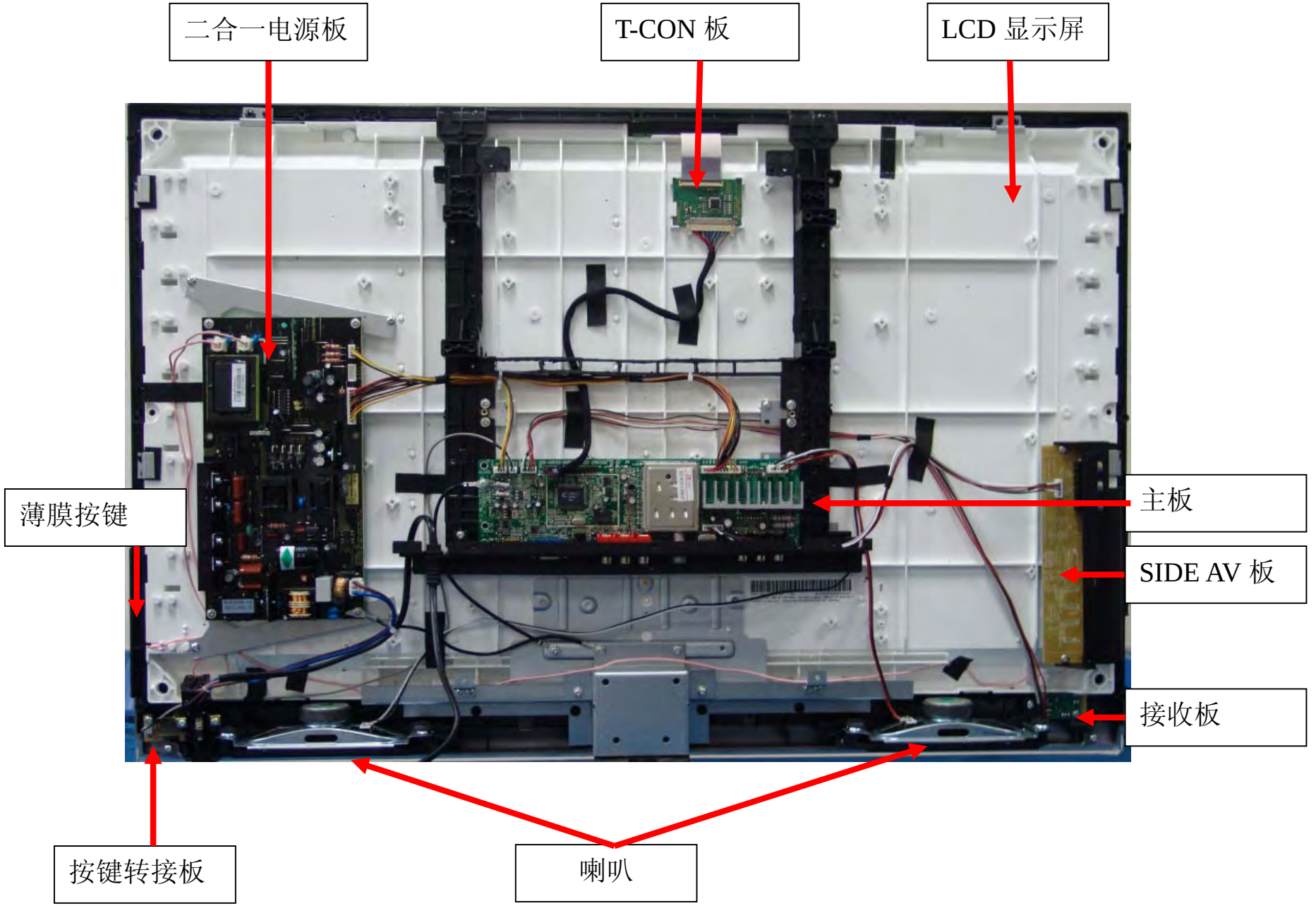


4.3 机内连接示意图

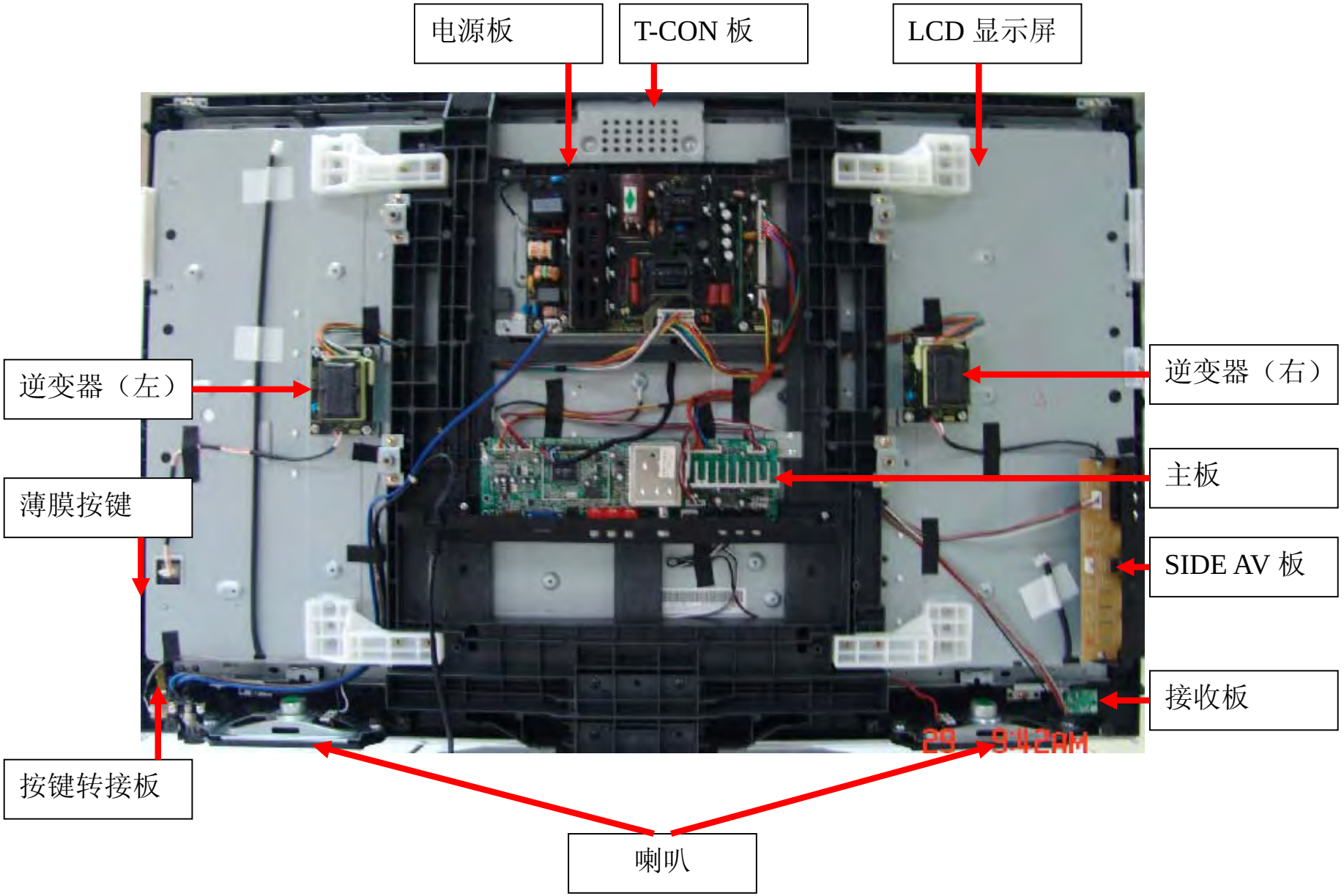
1、LCD26P08A



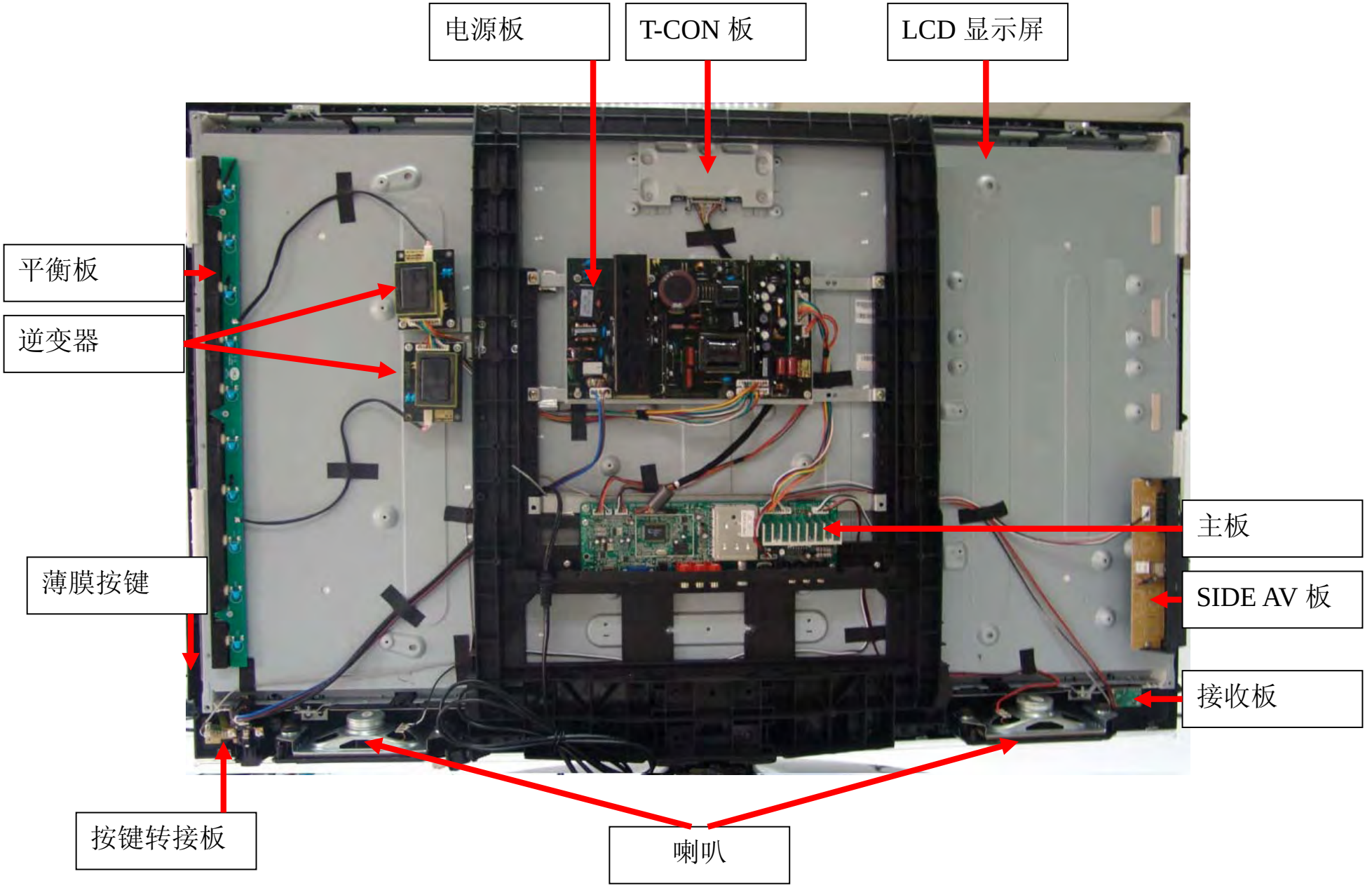
2．LCD32P08A



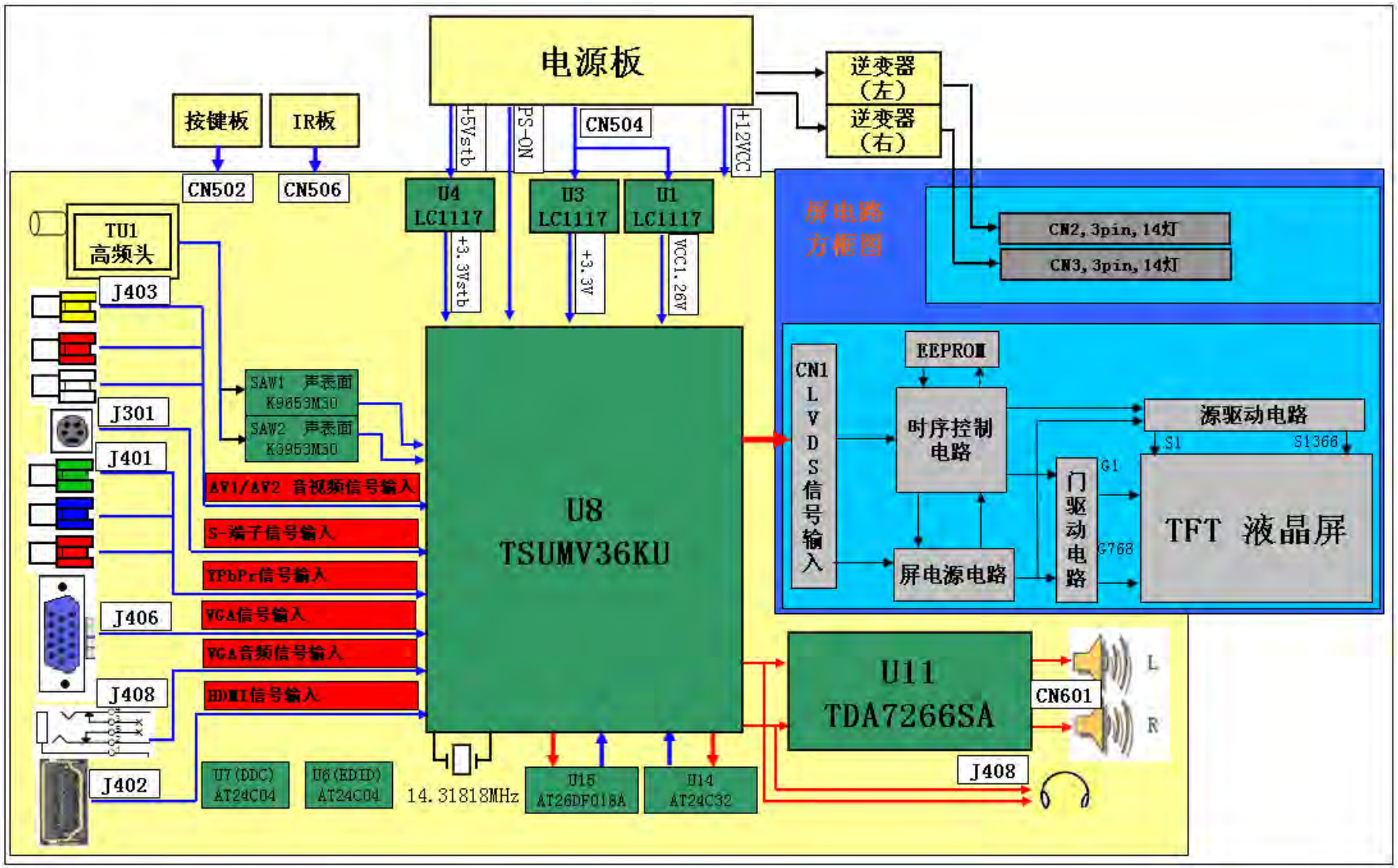
3．LCD37P08



3．LCD42P08A



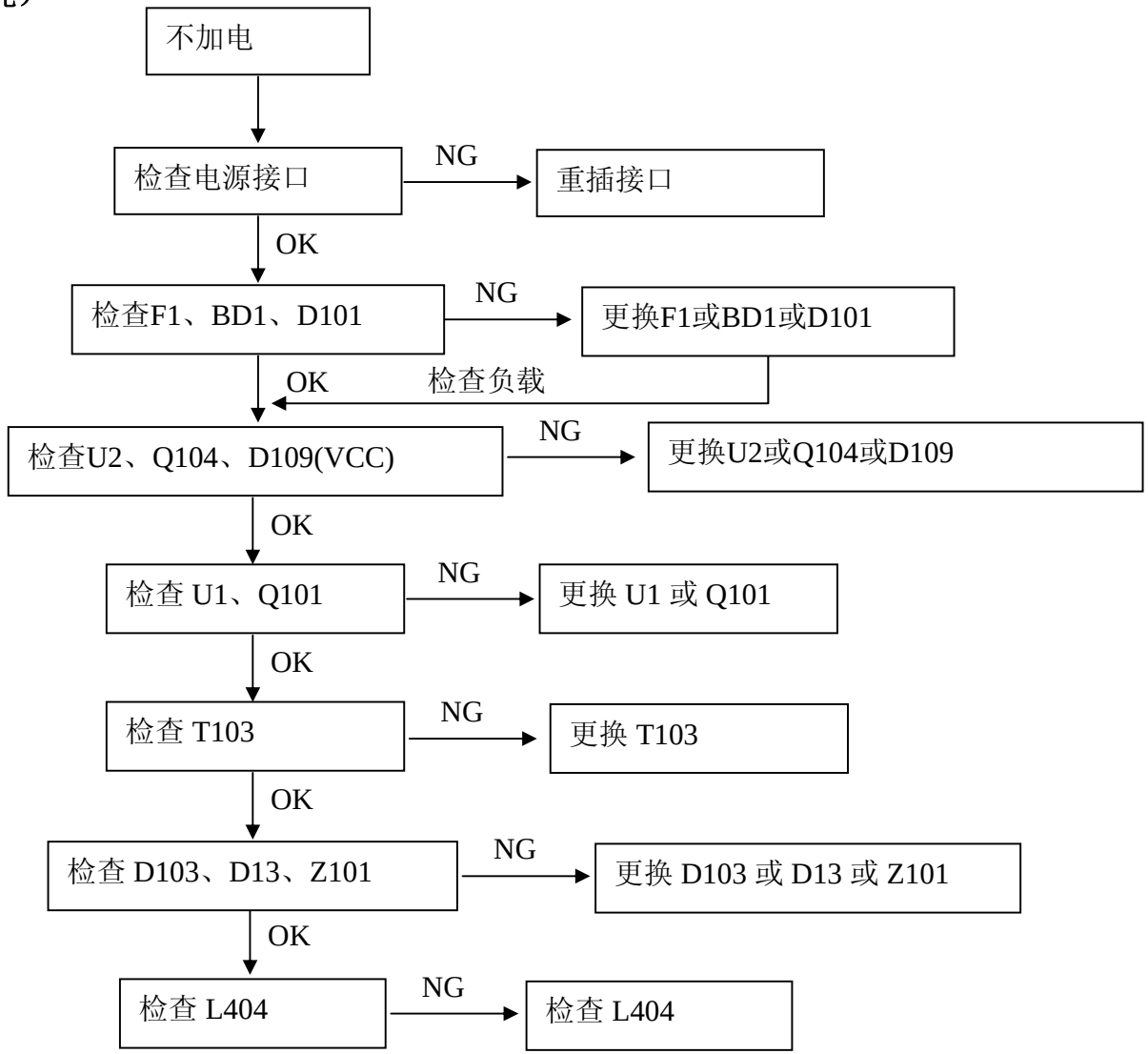
5. TV电气方框图


电源板
逆变器（左）
逆变器（右）
按键板
IR板
+5Vstb
PS-ON
CN504
+12VCC
CN502
CN506
U4 LC1117
U3 LC1117
U1 LC1117
+3.3Vstb
+3.3V
VCC1.26V
屏电路方框图
CN2,3pin,14灯
CN3,3pin,14灯
TU1 高频头
J403
J301
J401
J406
J408
J402
SAW1 声表面 K9653M30
SAW2 声表面 K3953M30
AV1/AV2 音视频信号输入
S-端子信号输入
YPbPr信号输入
VGA信号输入
VGA音频信号输入
HDMI信号输入
U8 TSUMV36KU
CN1 LVDS信号输入
EEPROM
时序控制电路
屏电源电路
门驱动电路
源驱动电路
S1
S1366
G1
G768
TFT 液晶屏
U11 TDA7266SA
CN601
L
R
J408
U7(DDC) AT24C04
U6(EDID) AT24C04
14.31818MHz
U15 AT26DF018A
U14 AT24C32

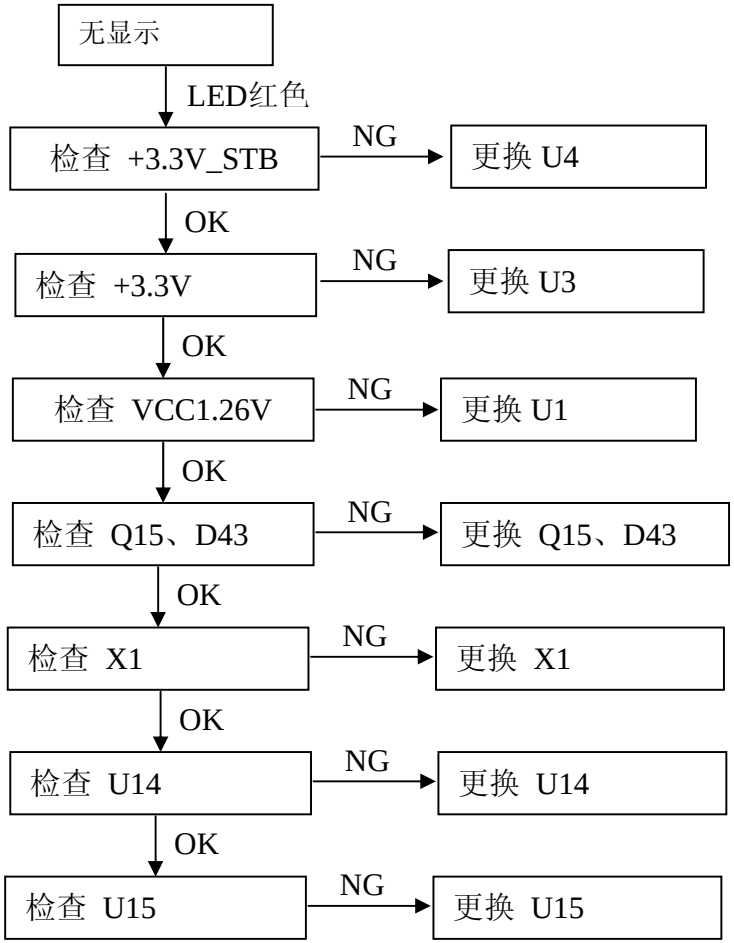
6. 故障处理流程

6.1板故障处理

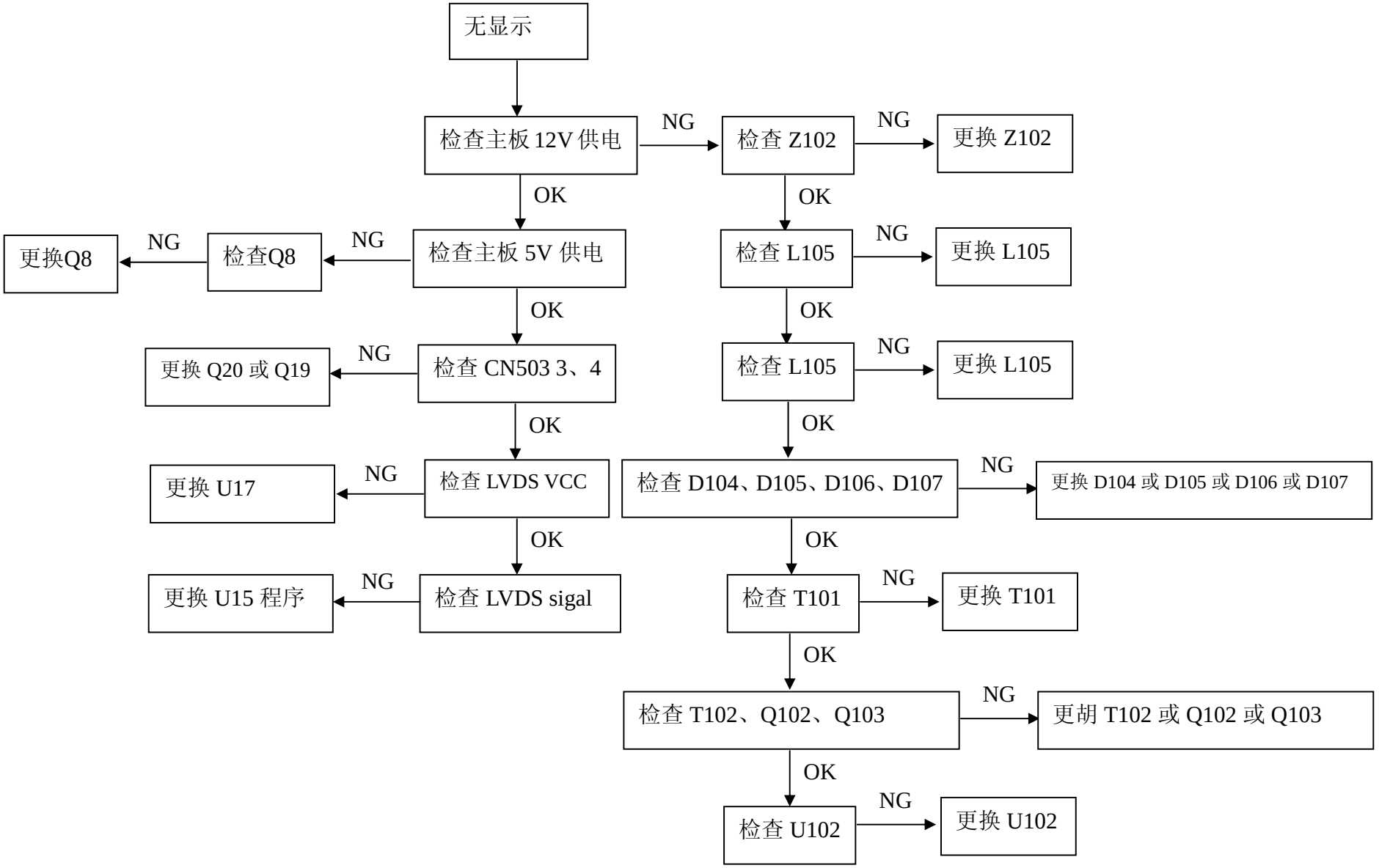
1、 无显示（LED不亮）



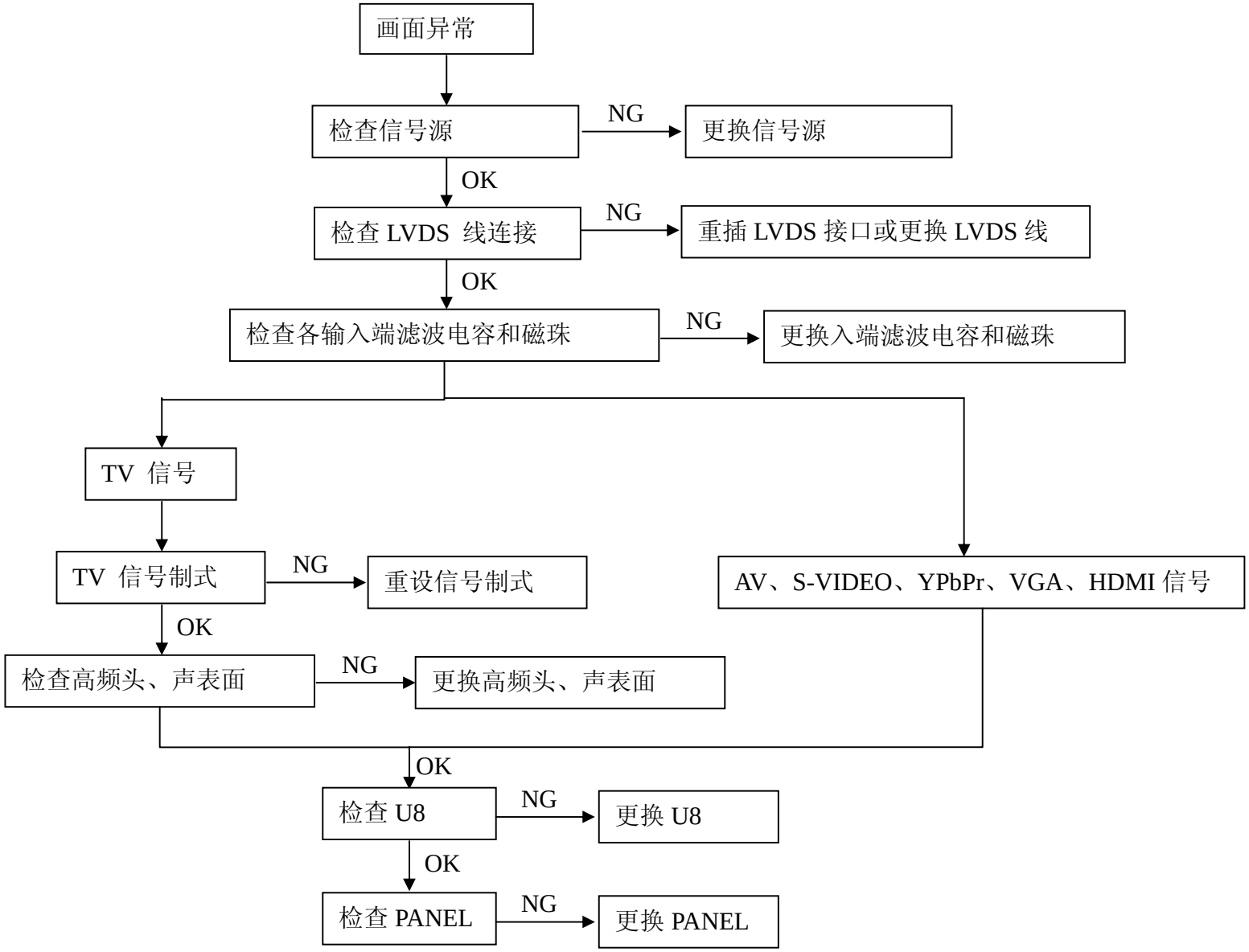
2、 无显示（LED亮红色灯）



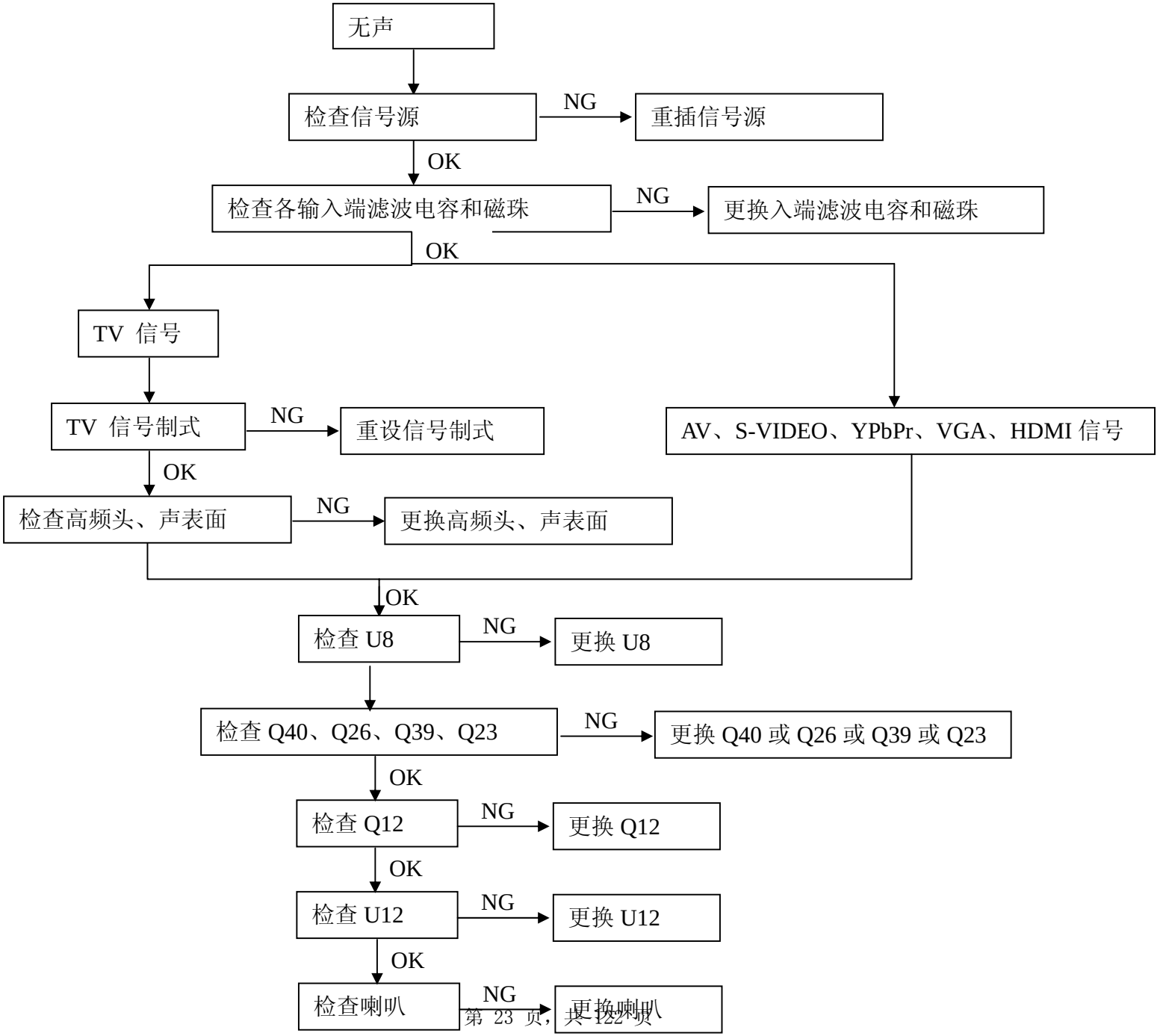
3、 无显示（LED不亮）


无显示
检查主板 12V 供电
NG
检查 Z102
NG
更换 Z102
OK
OK
更换Q8
NG
检查Q8
NG
检查主板 5V 供电
检查 L105
NG
更换 L105
OK
OK
更换 Q20 或 Q19
NG
检查 CN503 3、4
检查 L105
NG
更换 L105
OK
OK
更换 U17
NG
检查 LVDS VCC
检查 D104、D105、D106、D107
NG
更换 D104 或 D105 或 D106 或 D107
OK
OK
更换 U15 程序
NG
检查 LVDS sigal
检查 T101
NG
更换 T101
OK
检查 T102、Q102、Q103
NG
更胡 T102 或 Q102 或 Q103
OK
检查 U102
NG
更换 U102

4、 画面异常


画面异常
检查信号源
NG
更换信号源
OK
检查 LVDS 线连接
NG
重插 LVDS 接口或更换 LVDS 线
OK
检查各输入端滤波电容和磁珠
NG
更换入端滤波电容和磁珠
TV 信号
TV 信号制式
NG
重设信号制式
OK
检查高频头、声表面
NG
更换高频头、声表面
AV、S-VIDEO、YPbPr、VGA、HDMI 信号
OK
检查 U8
NG
更换 U8
OK
检查 PANEL
NG
更换 PANEL

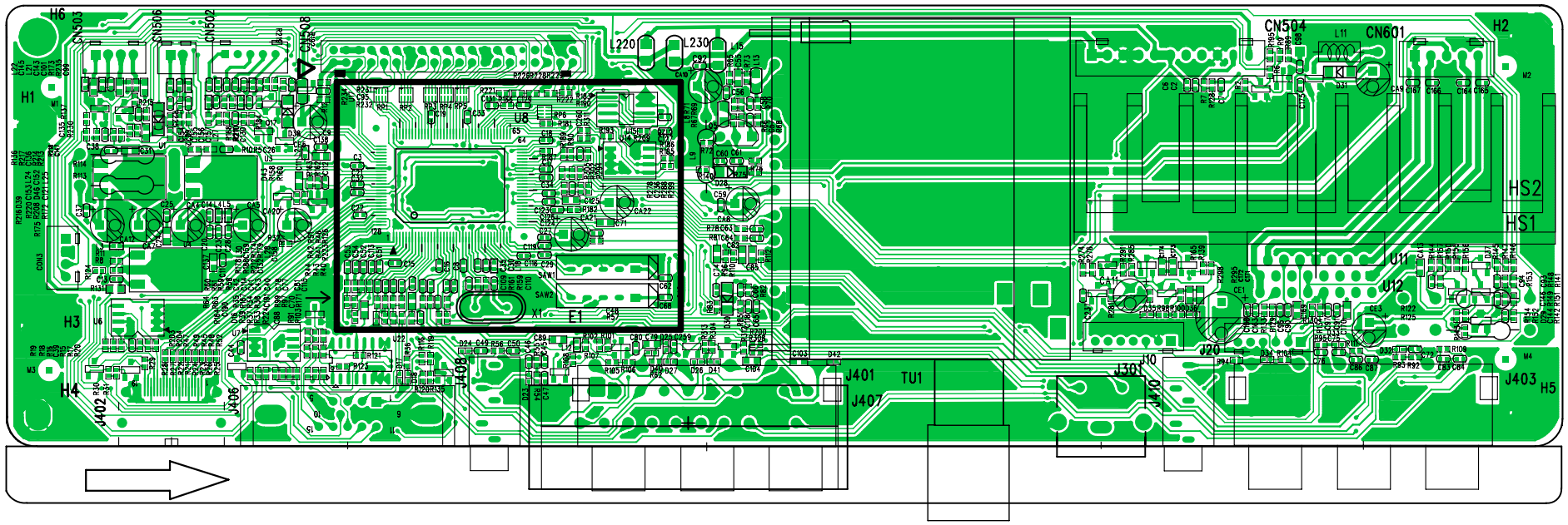
5、 无声

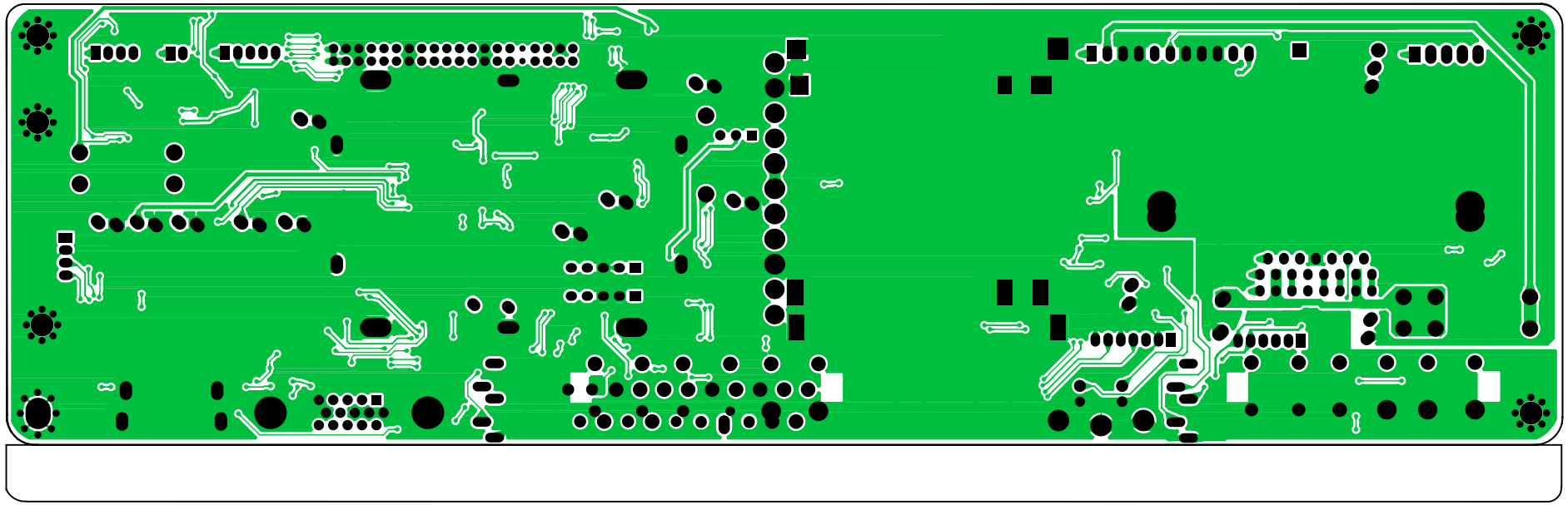

无声
检查信号源
NG
重插信号源
OK
检查各输入端滤波电容和磁珠
NG
更换入端滤波电容和磁珠
OK
TV 信号
TV 信号制式
NG
重设信号制式
OK
检查高频头、声表面
NG
更换高频头、声表面
AV、S-VIDEO、YPbPr、VGA、HDMI 信号
OK
检查 U8
NG
更换 U8
检查 Q40、Q26、Q39、Q23
NG
更换 Q40 或 Q26 或 Q39 或 Q23
OK
检查 Q12
NG
更换 Q12
OK
检查 U12
NG
更换 U12
OK
检查喇叭
NG
更换喇叭

5 PCB LAYOUT

5.1 主板

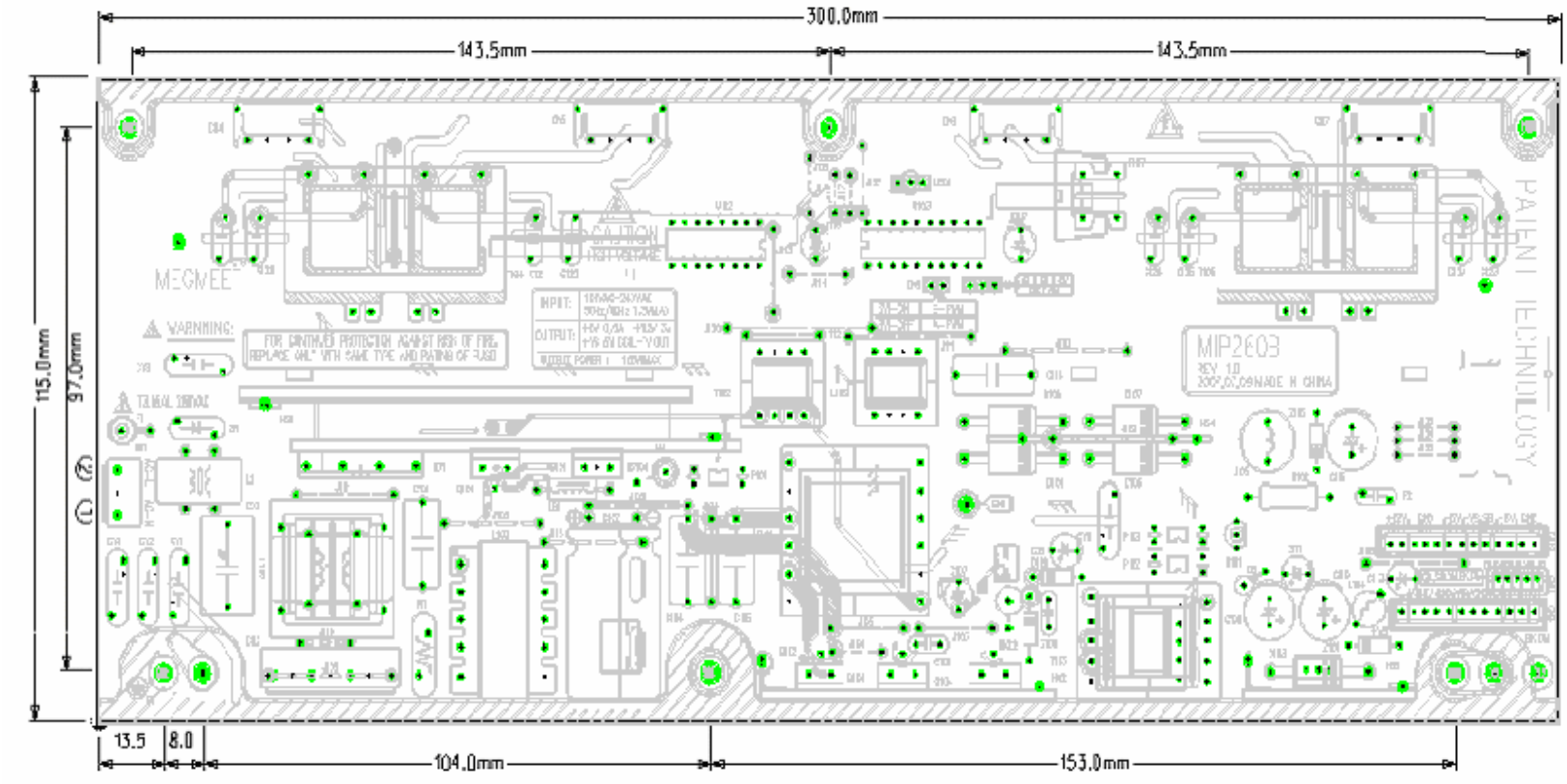
正面视图





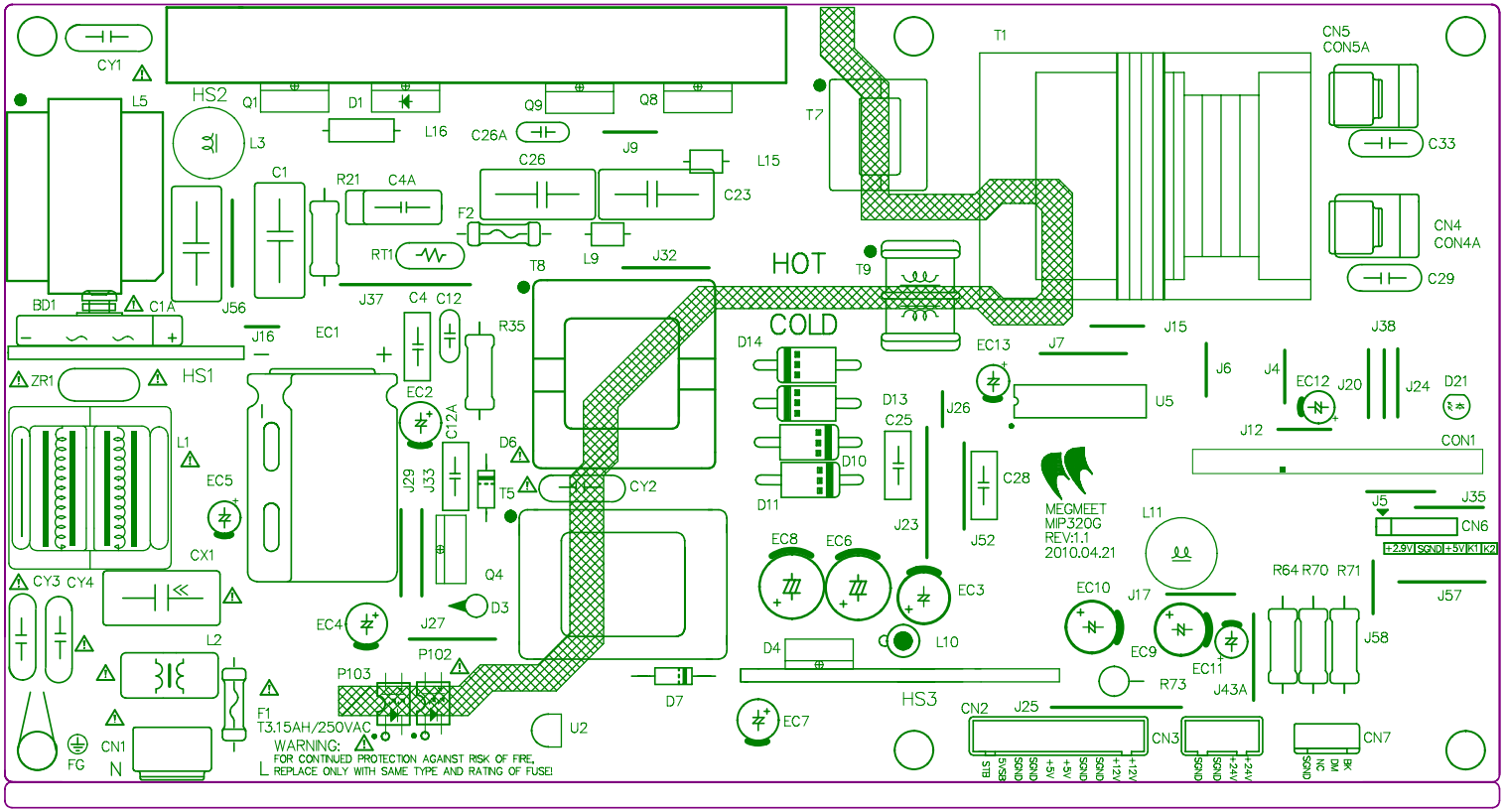
5.2 电源板

1.MIP260B-19(LCD26P08A)

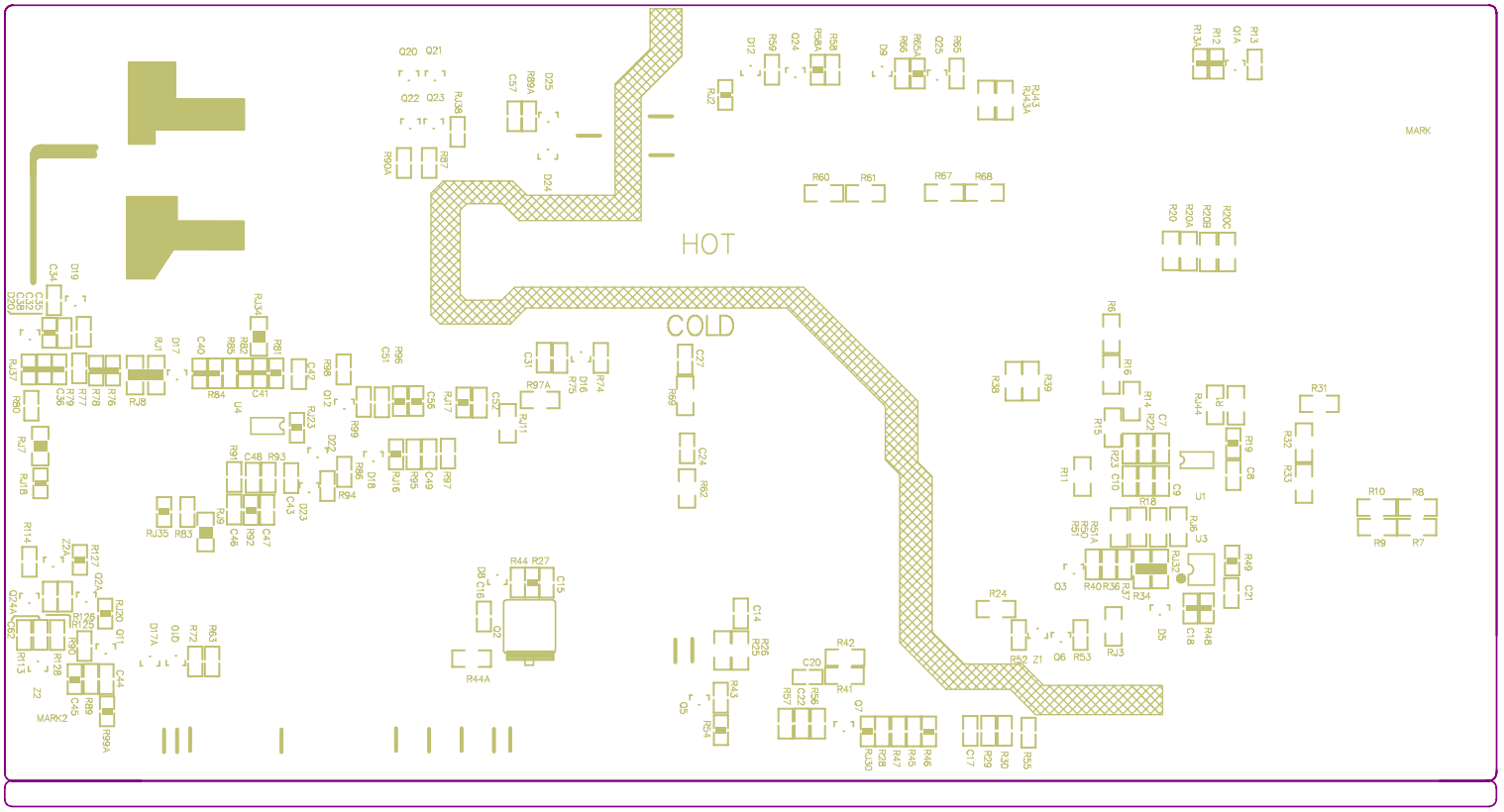


2、MIP320G-A(LCD32P08A)

1） TOP

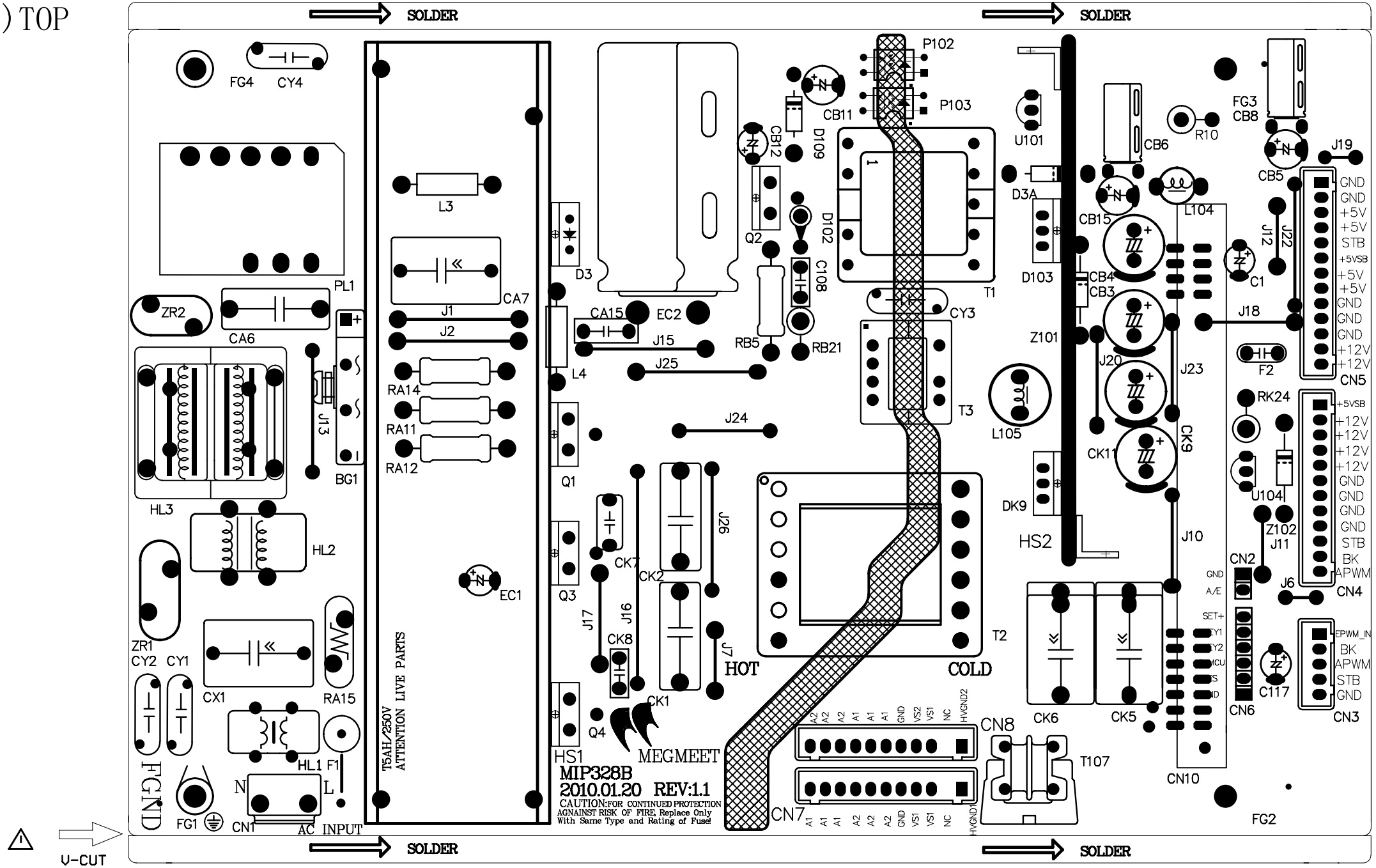


2)BOTTOM

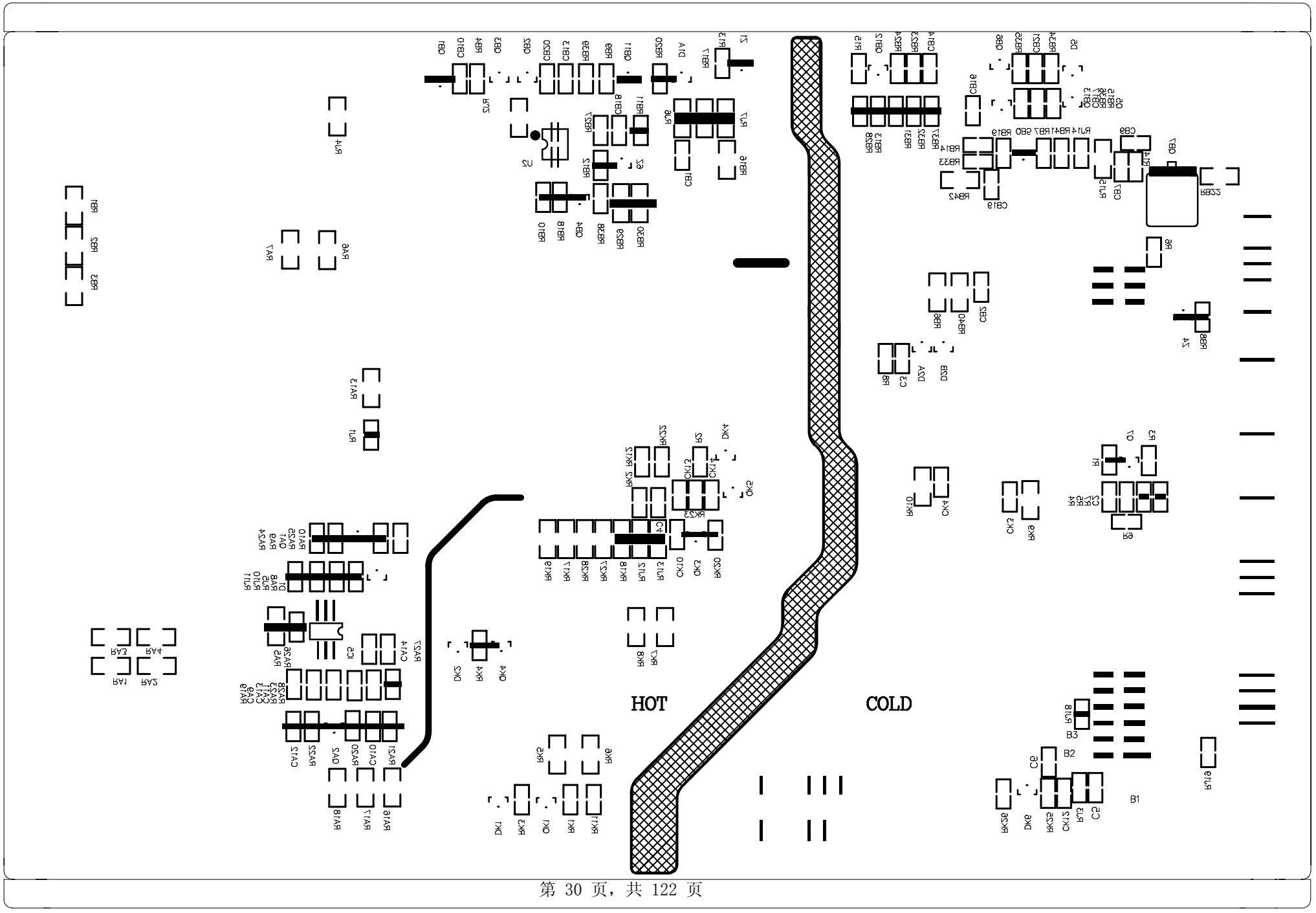


3、MIP328B-K-1(LCD37P08)

1)TOP

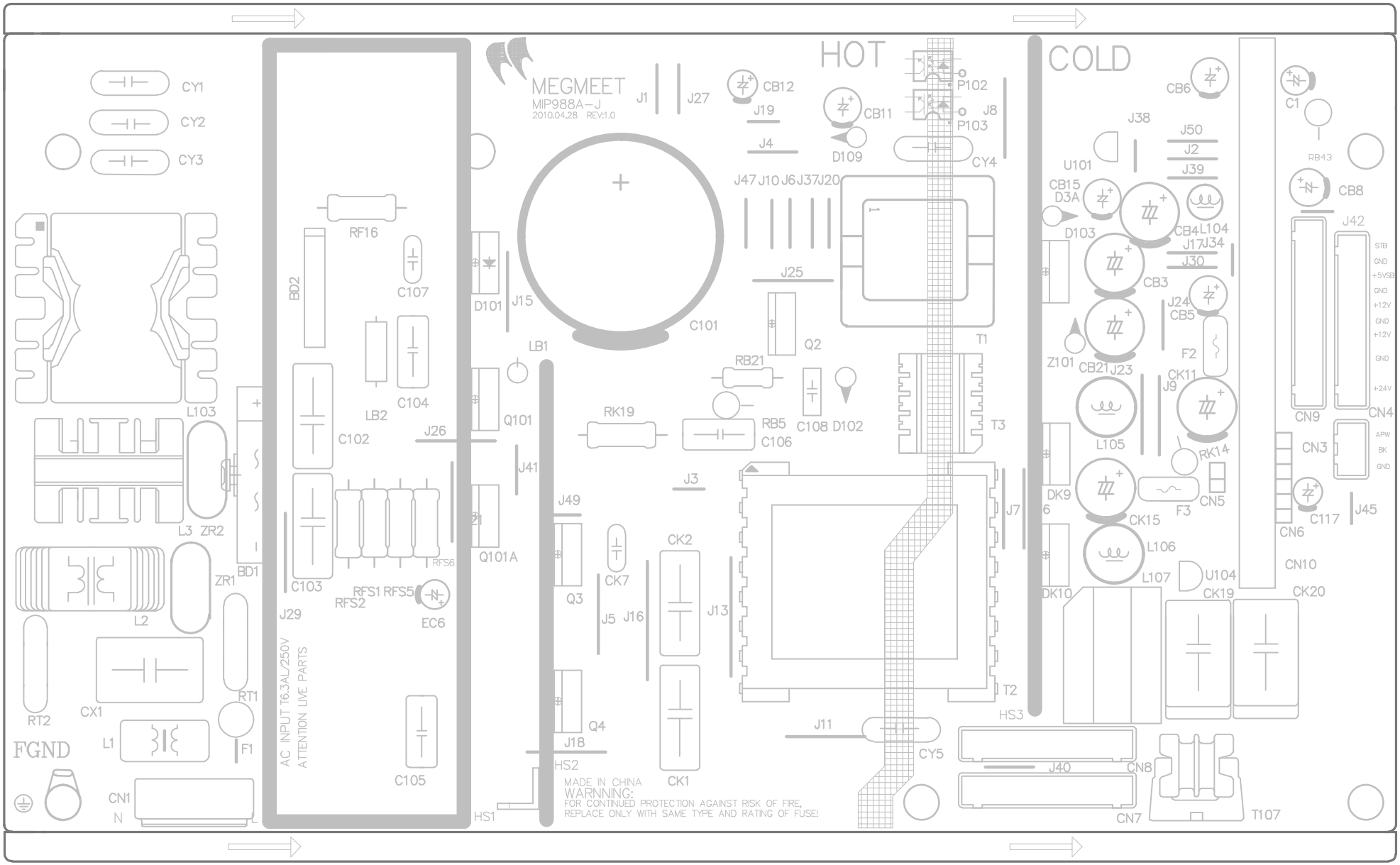


2) BOTTOM

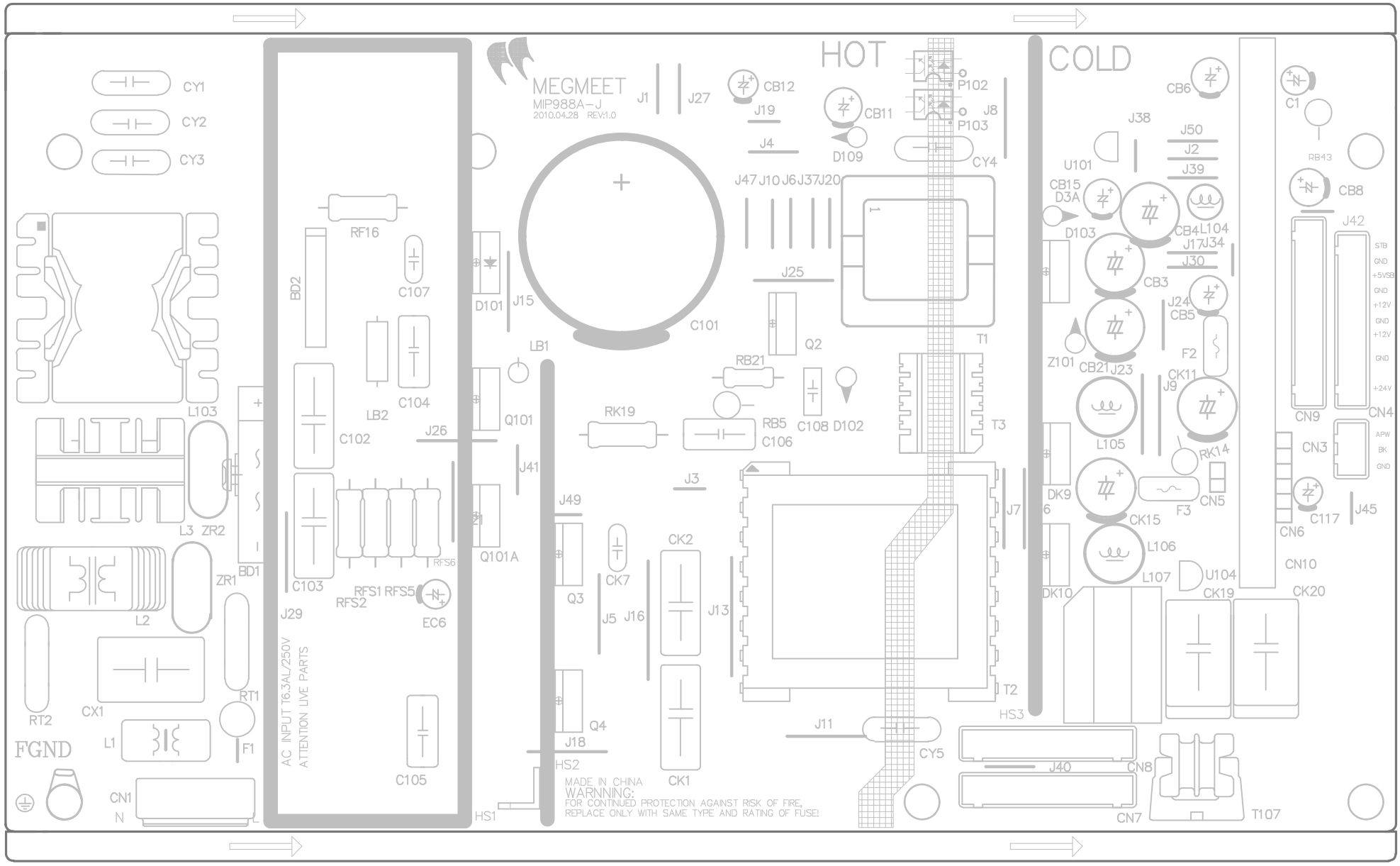


4、MIP988A-J（LCD42P08A）

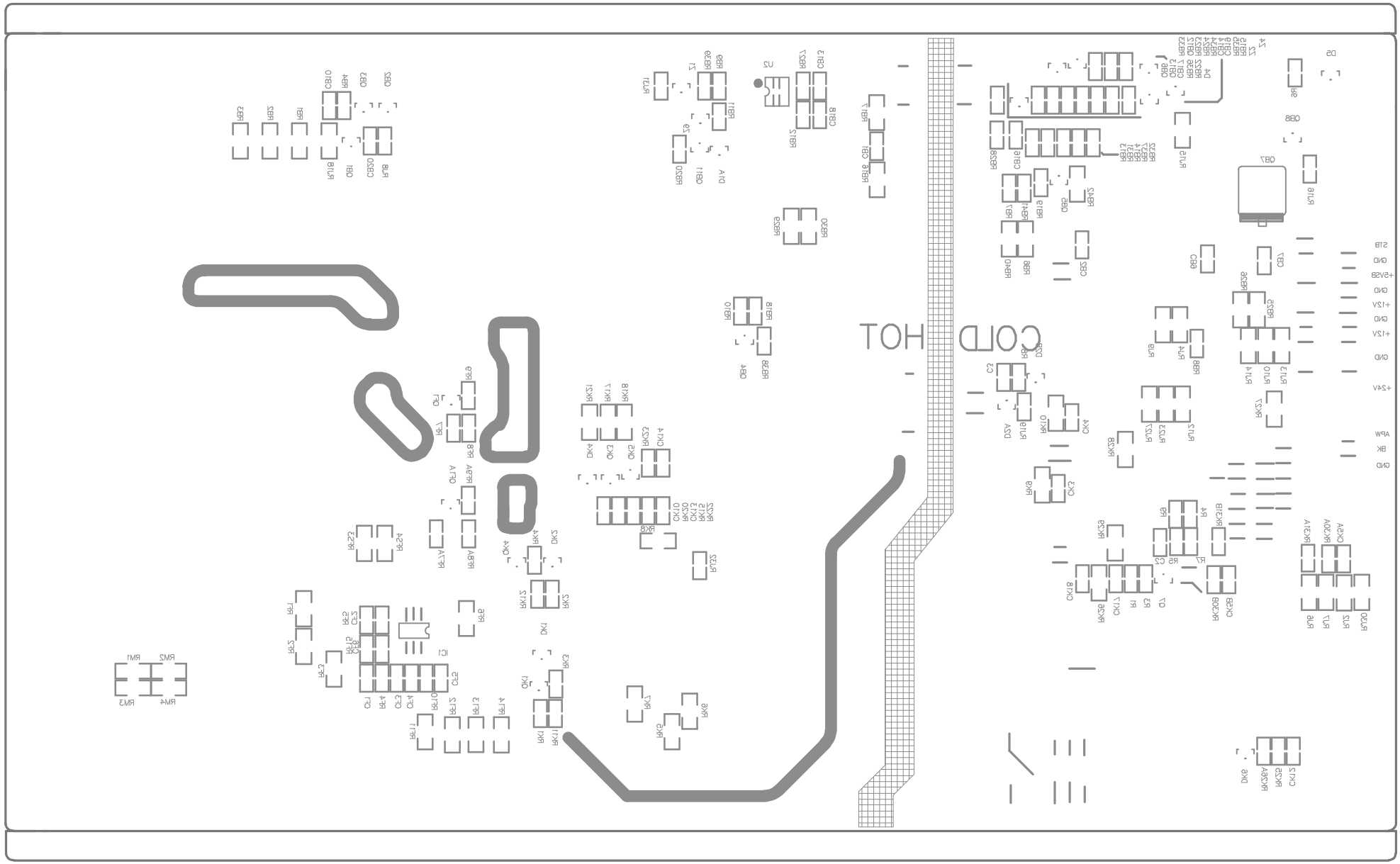
1)TOP



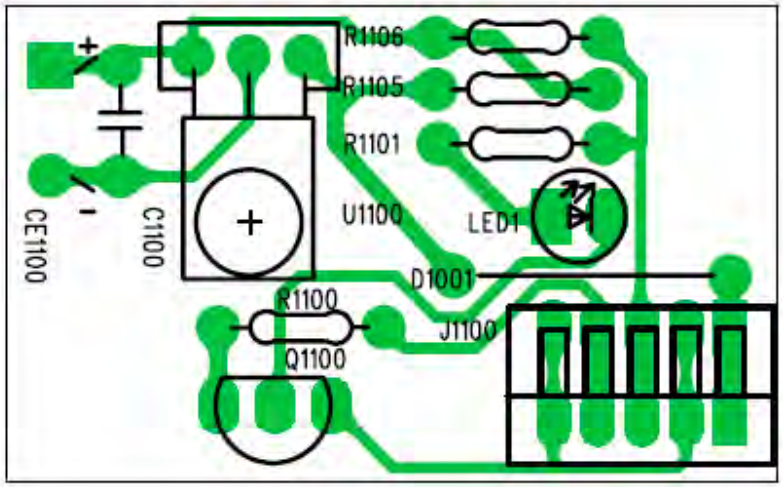
2)BOTTOM


MEGMEET
MIP988A-J
2010.04.28 REV:1.0
HOT
COLD
AC INPUT T6.3AL/250V
ATTENTION LIVE PARTS
FGND
MADE IN CHINA
WARNNING:
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE,
REPLACE ONLY WITH SAME TYPE AND RATING OF FUSE!
CY1
CY2
CY3
RF16
BD2
C107
D101
J15
LB1
C101
J25
Q2
T1
RB21
RB5
C106
C108
D102
RK19
C104
LB2
C102
J26
Q101
Q101A
J41
J49
J3
L103
L3
ZR2
BD1
ZR1
L2
C103
RFS1
RFS2
RFS5
RFS6
EC6
J29
Q3
CK7
J5
J16
CK2
J13
T3
J7
T2
HS3
Q4
J18
HS2
HS1
CK1
J11
CY5
J40
CN8
CN7
T107
RT2
CX1
RT1
L1
F1
CN1
N
L
C105
J1
J27
CB12
J19
J4
CB11
D109
P102
P103
J8
CY4
J47
J10
J6
J37
J20
U101
CB15
D3A
D103
Z101
CB21
J23
CB6
J38
J50
J2
J39
CB4
L104
J17
J34
J30
CB3
J24
CB5
F2
CK11
J9
L105
RK14
CN5
F3
DK9
6
CK15
L106
L107
DK10
U104
CK19
CK20
CN10
C1
RB43
CB8
J42
CN9
CN4
CN3
C117
J45
CN6
STB
GND
+5VSB
GND
+12V
GND
+12V
GND
+24V
APW
BK
GND

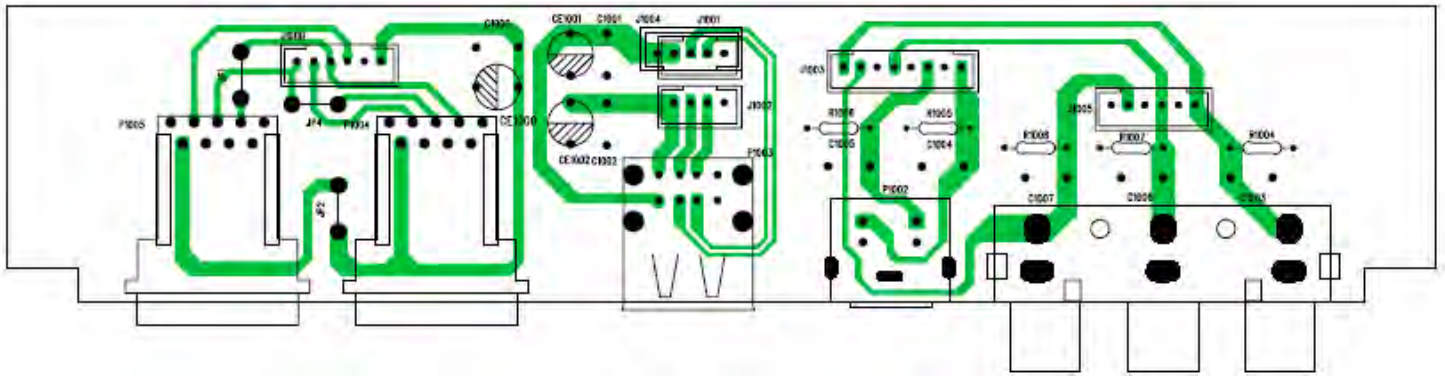
2)BOTTOM



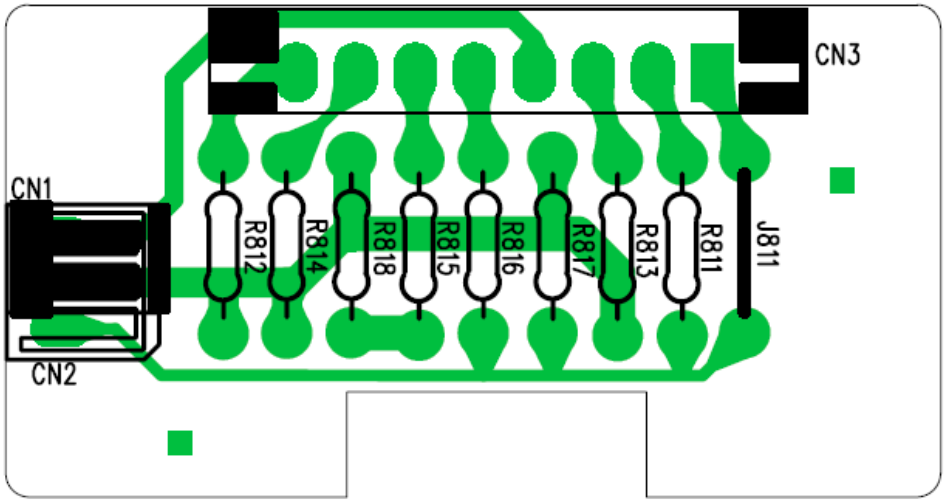
5.3 IR板

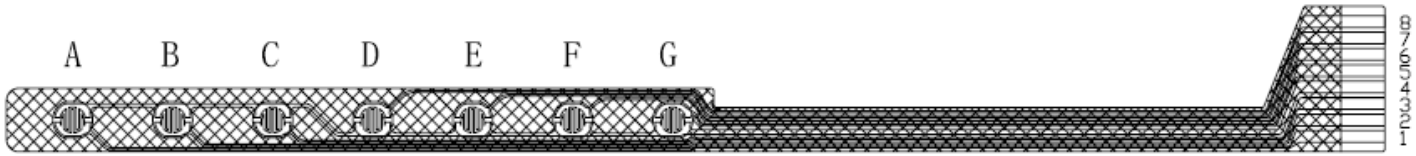


5.4 SIDE AV板



5.5 按键转接板与薄膜按键





阴影部分丝印绿色阻焊

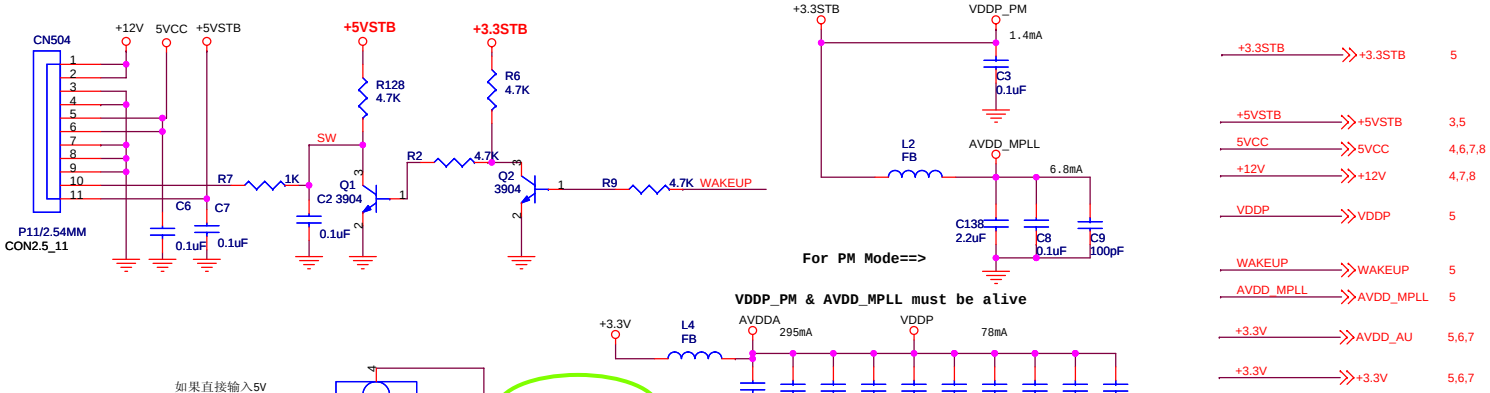
连接关系

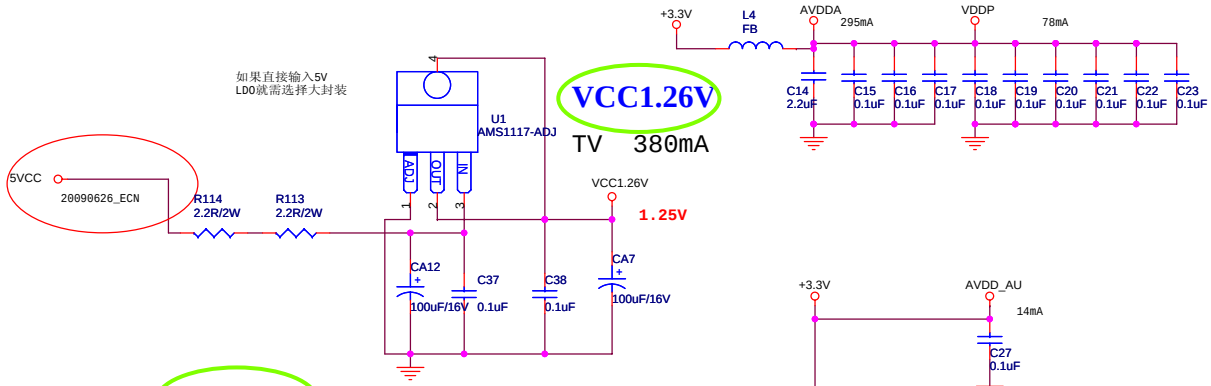
4 为总线	A	B	C	D	E	F	G
	1	2	3	8	7	6	5

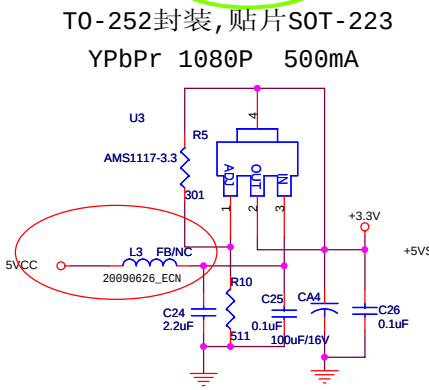
7 电路图

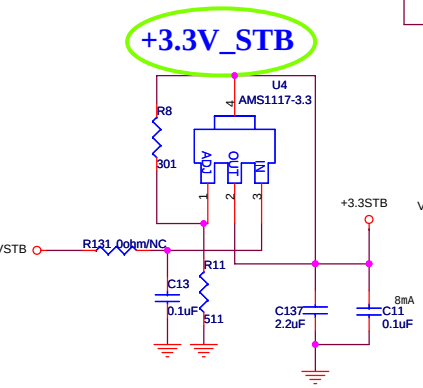
7.1 主板

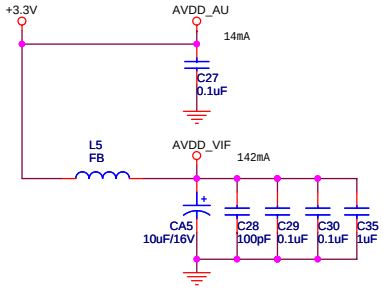
1) Power

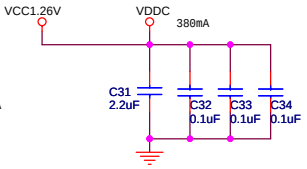












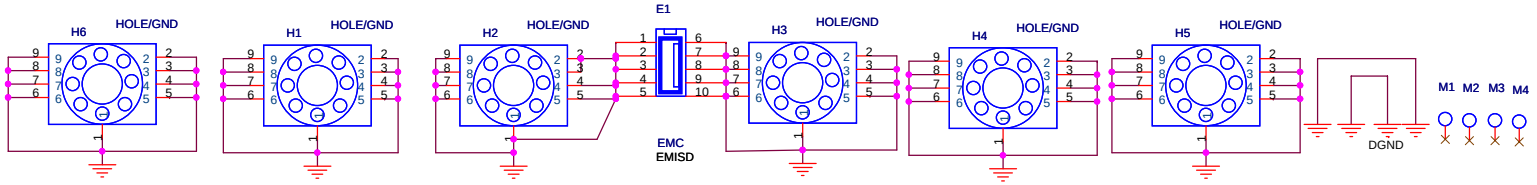
GPIO Define

PIN115: Standby Power WAKEUP
PIN77 GPIOD0: LED CONTROL G
PIN76 GPIOD1: SCART ENABLE SC_EN
PIN70 AD1: 24C32 EEPROT WITE PROTEL
PIN71 AD0: Audio AMP Mute

PIN59 PWM3: 12V BOOT TO 40VDC
PIN60 PWM2: FLASH WP
PIN62 PWM0: Backlight Diming Control
PIN66 RDZ: LVDS Power Switching
PIN67 WRZ: Backlight ON/OFF Control
PIN68 AD2: I2C_SCL
PIN69 AD3: I2C_SDA
PIN65 ALE: NO USE
PIN106 IRIN: IR_SYNC
PIN107 SAR2: 4052_CTL
PIN108 SAR1: KEYPADS control2
PIN109 SAR0: KEYPADS control1

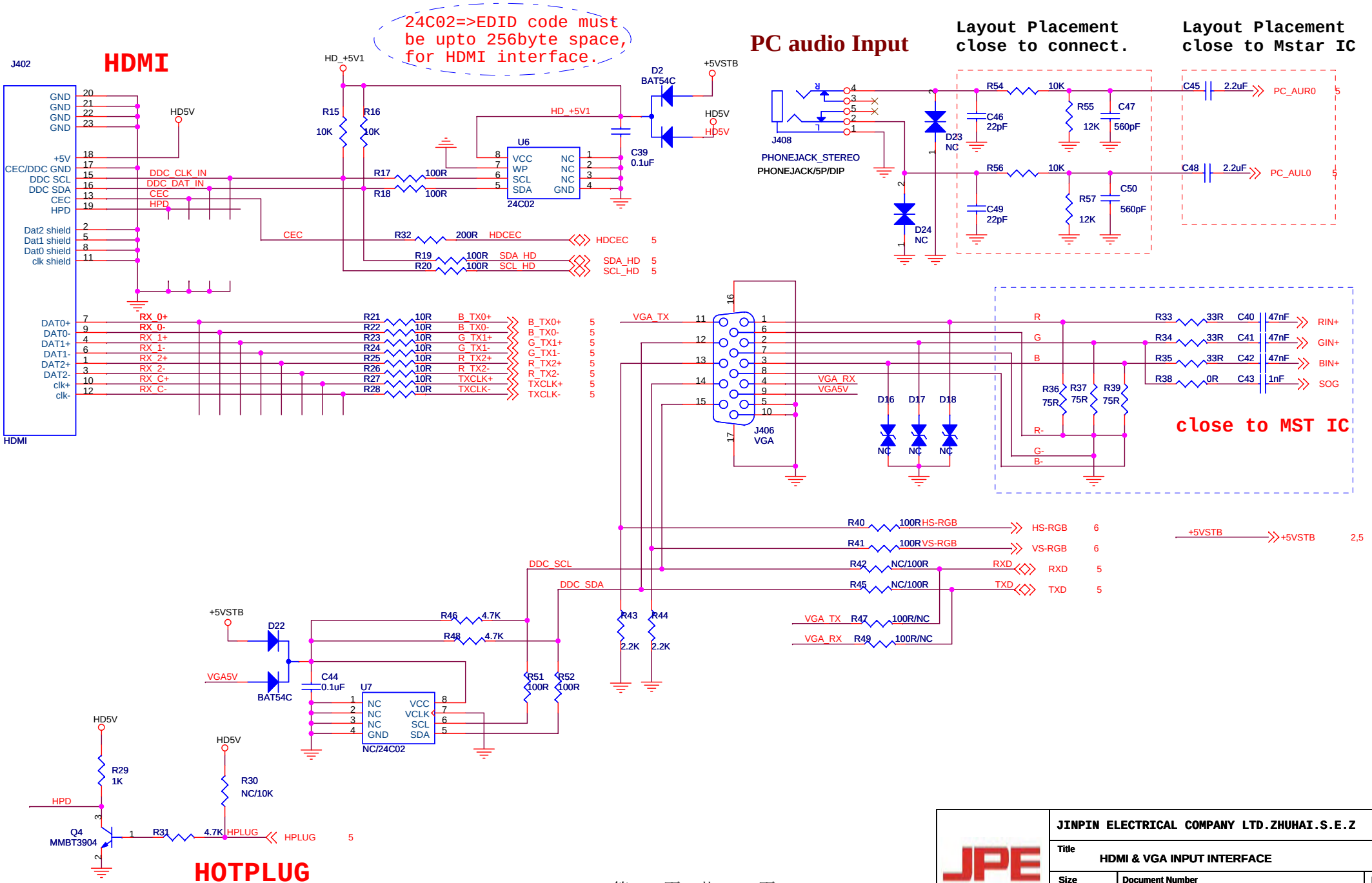
PIN114: HDCEC
PIN126: HDMI HOT PLUG HPLUG

Schematics pages list:



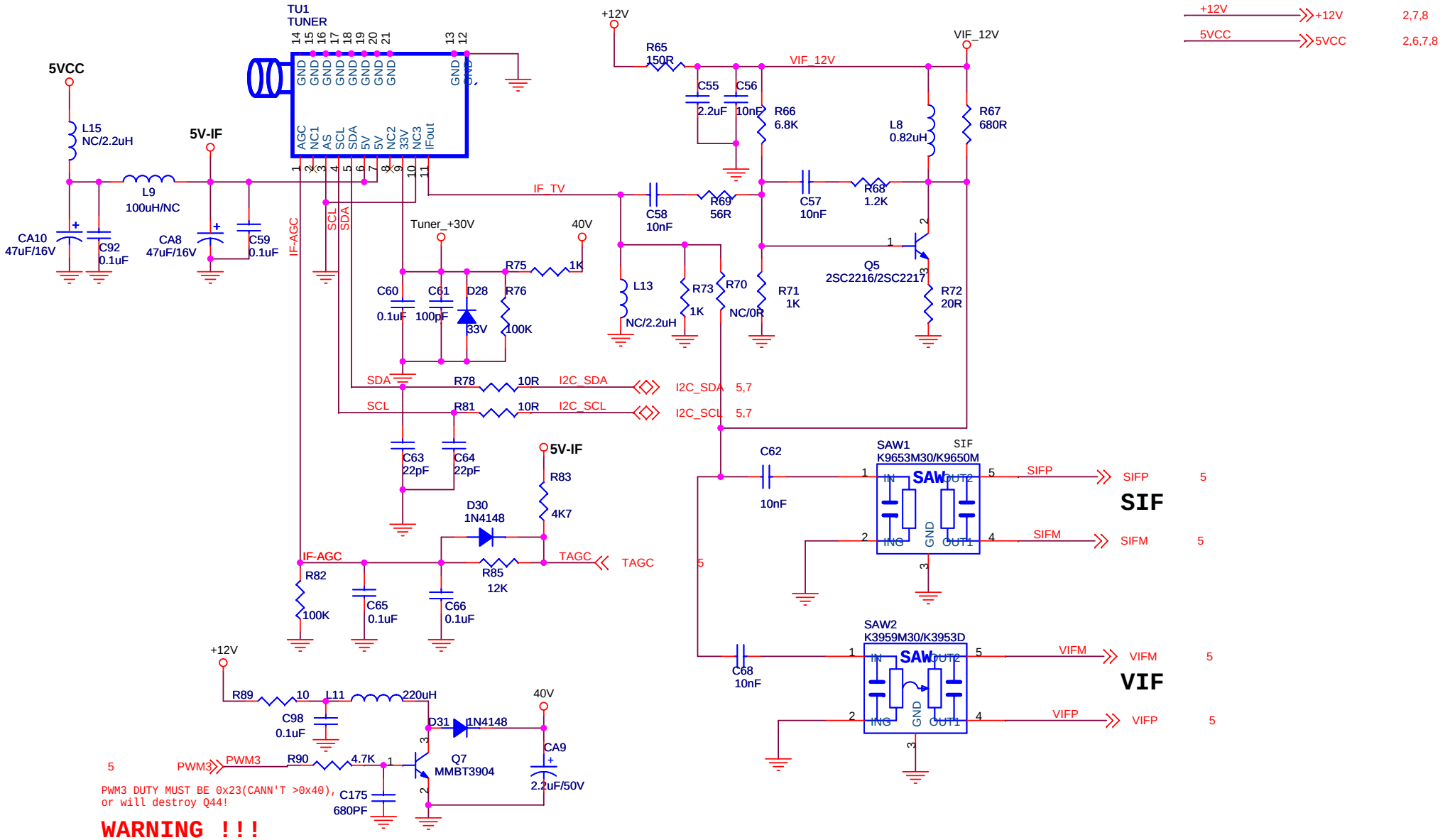
JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z			
Title: POWER			
Size: Custom	Document Number: JPE_36KURW_V01		Rev: 01
Draw: Zhangwd	Date: Wednesday, July 28, 2010	Sheet 2 of 8	

2)HDMI&VGA INPUT INTERFACE



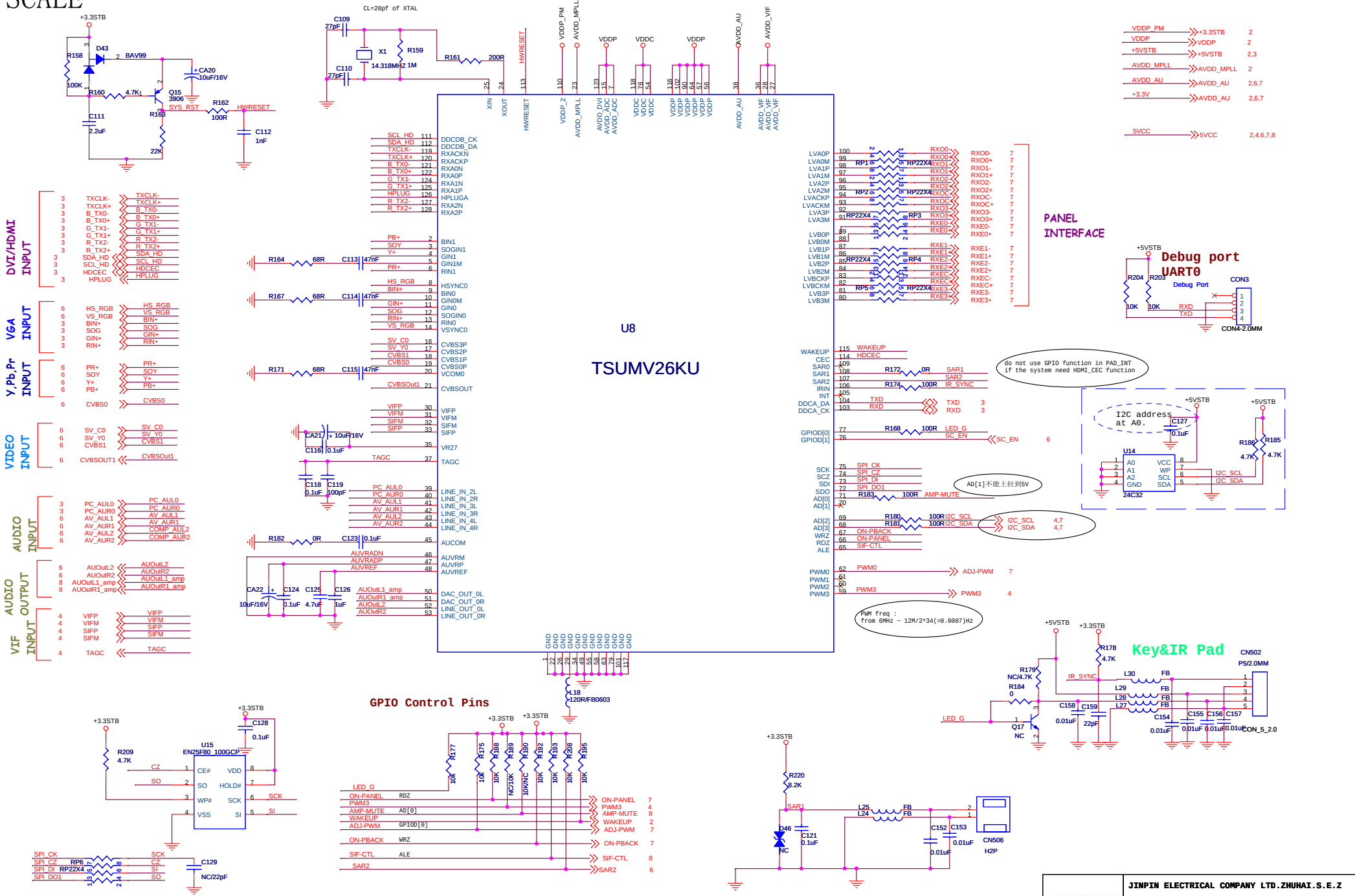
JPE	JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z	
	Title: HDMI & VGA INPUT INTERFACE	
	Size: Custom	Document Number: JPE_36KURW_V01 Rev: 01
	Draw: Zhangwd	Date: Friday, January 22, 2010 Sheet 3 of 8

3) IF INTERFACE



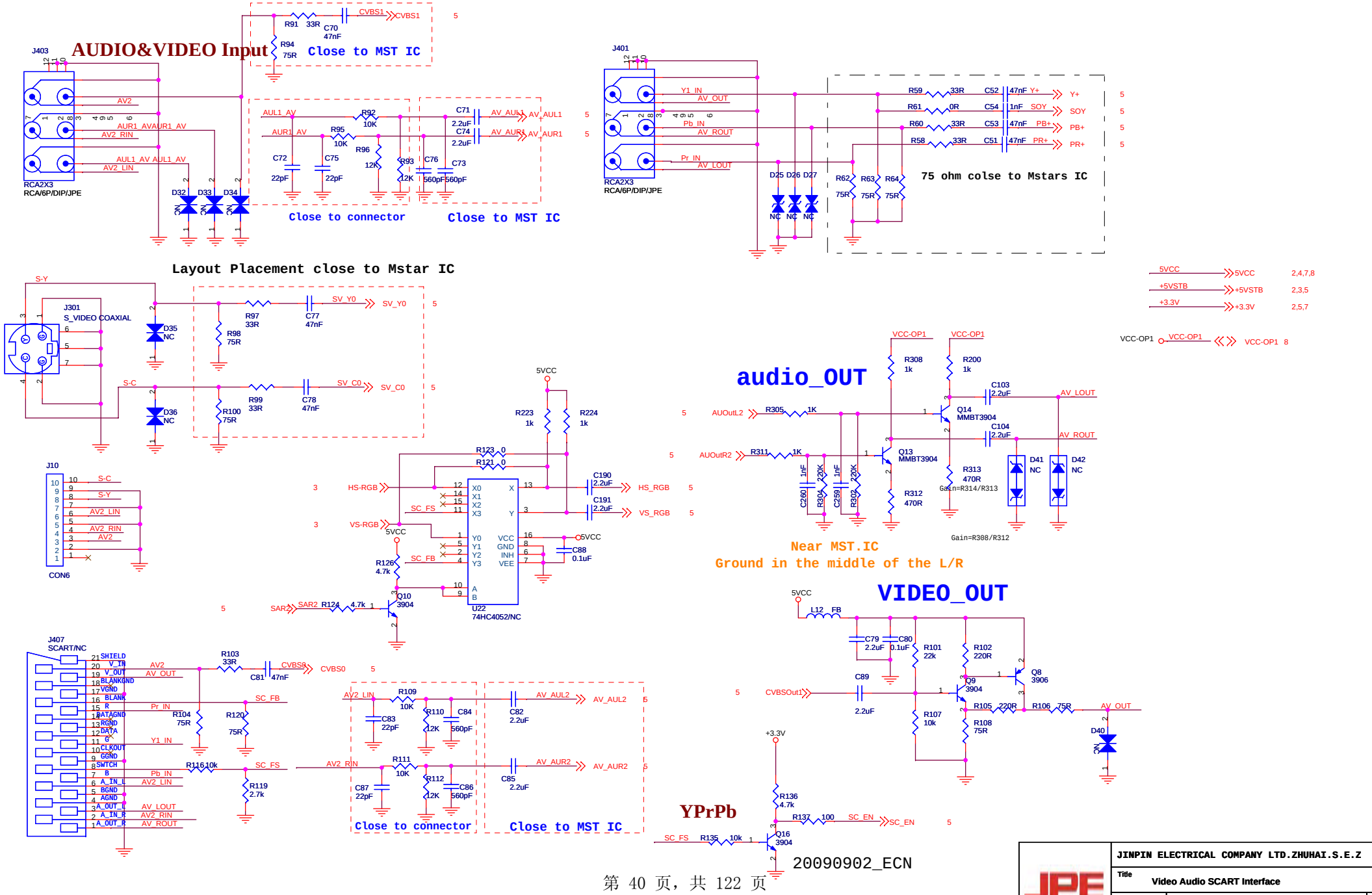
JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z		
Title: IF Interface		
Size: Custom	Document Number: JPE_36KURW_V01	Rev: 01
Draw: Zhangwd	Date: Wednesday, July 28, 2010	Sheet 4 of 8

4) SCALE



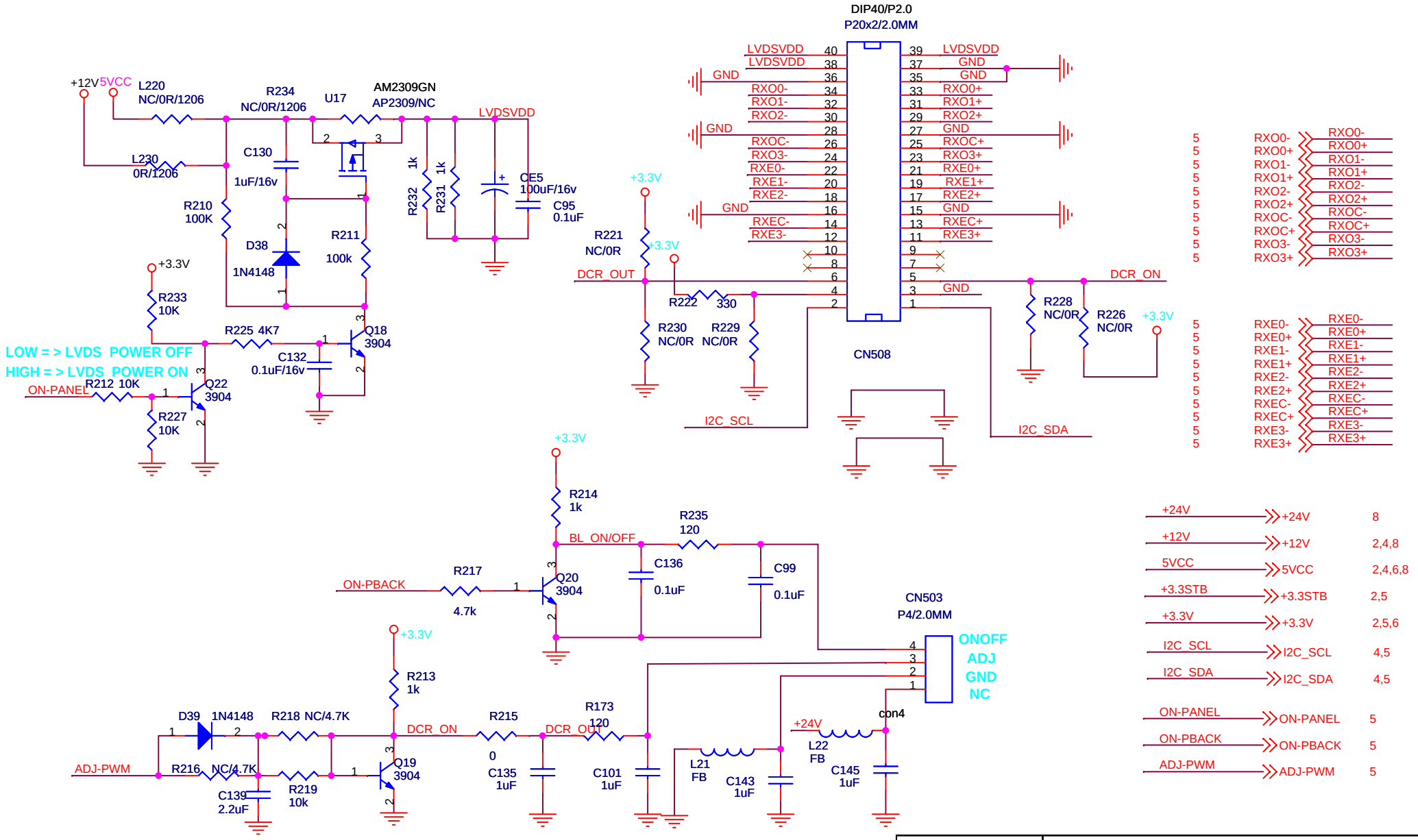
JPE	JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z	
	Title: SCALE	
	Size: Custom	Document Number: JPE_36KURW_V01 Rev: 01
	Draw: Zhangwd	Date: Friday, January 15, 2010 Sheet 5 of 8

5)VIDEO&AUDIO



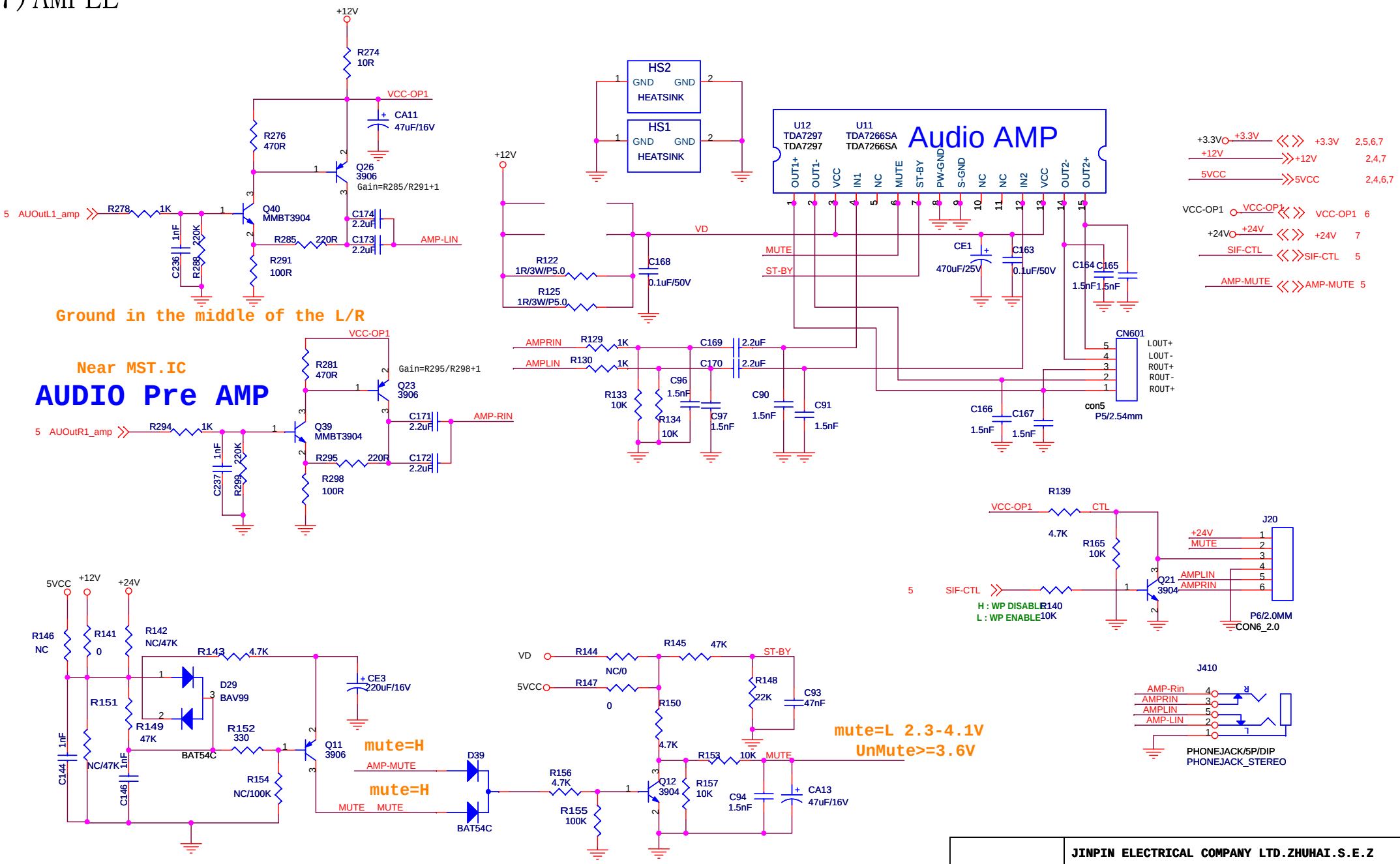
JPE	JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z	
	Title: Video Audio SCART Interface	
	Size: Custom	Document Number: JPE_36KURW_V01 Rev: 01
	Draw: Zhangwd	Date: Thursday, January 14, 2010 Sheet 6 of 8

6) PANEL



JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z		
Title: PANEL I/F		
Size: Custom	Document Number: JPE_36KURW_V01	Rev: 01
Draw: Zhangwd	Date: Wednesday, July 28, 2010	Sheet 7 of 8

7) AMPLE

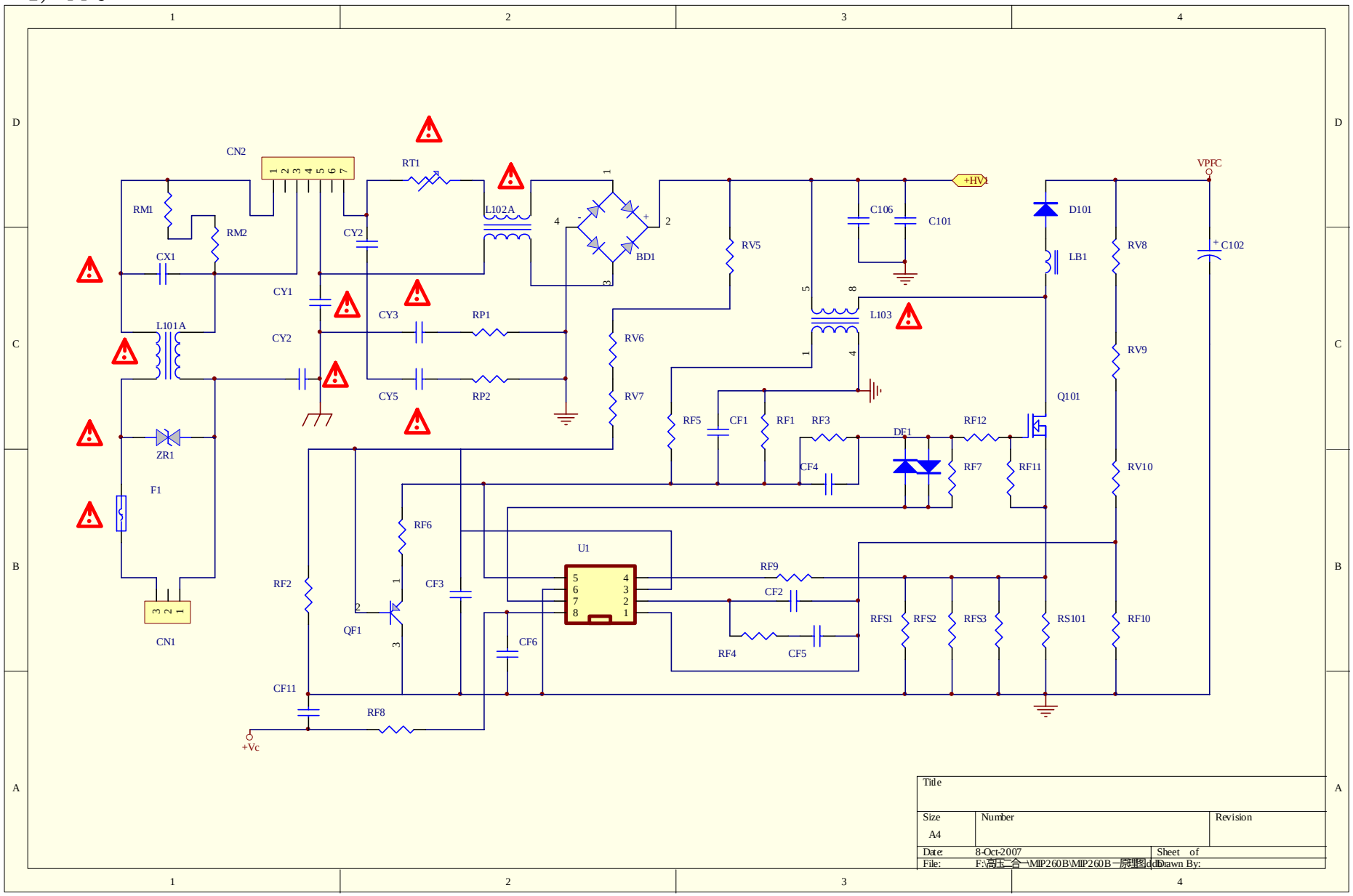


JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z		
Title: AMP		
Size: Custom	Document Number: JPE_36KURW_V01	Rev: 01
Draw: Zhangwd	Date: Wednesday, July 28, 2010	Sheet 8 of 8

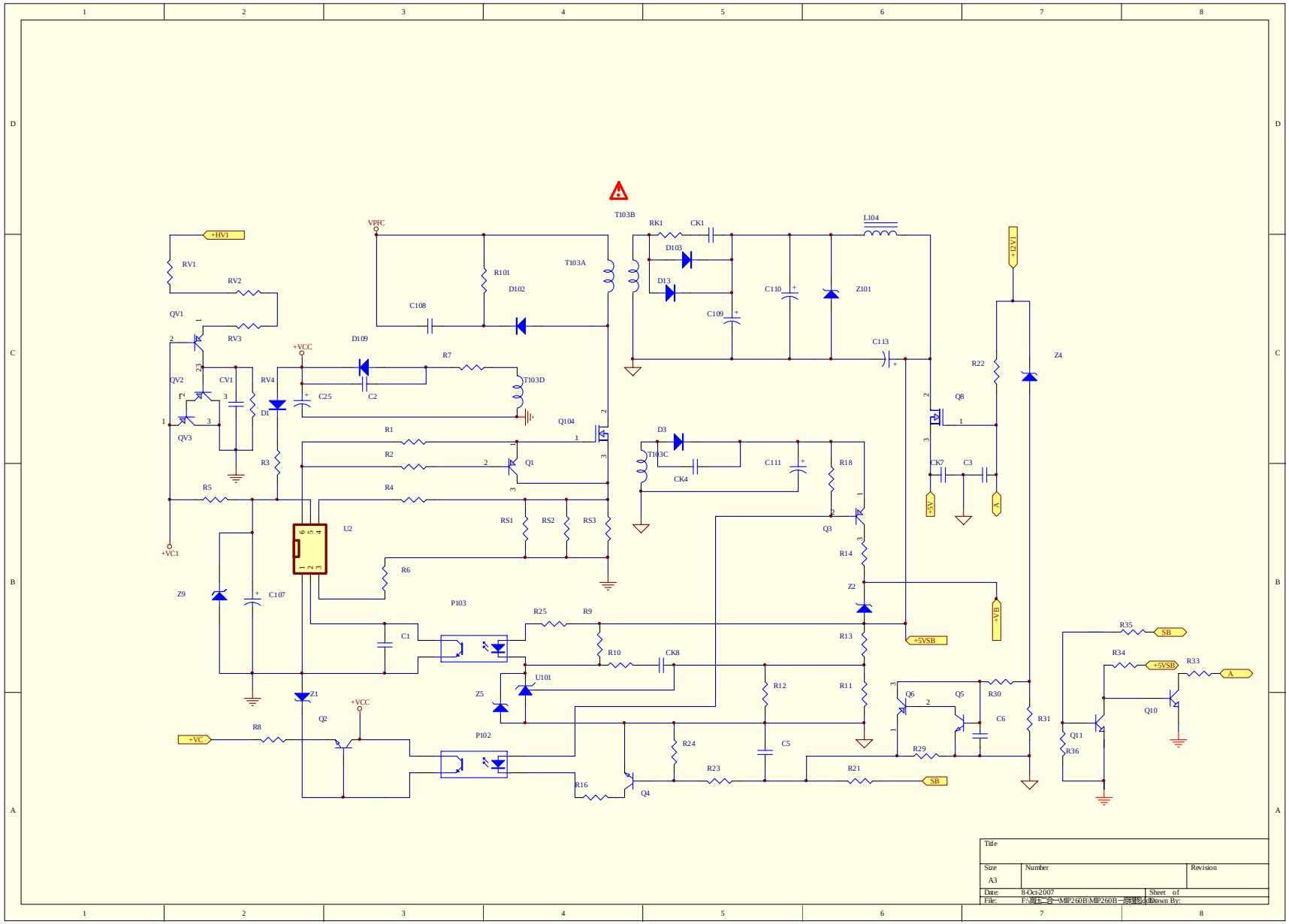
7.2 电源板

1. MIP26B-19(LCD26P08A)

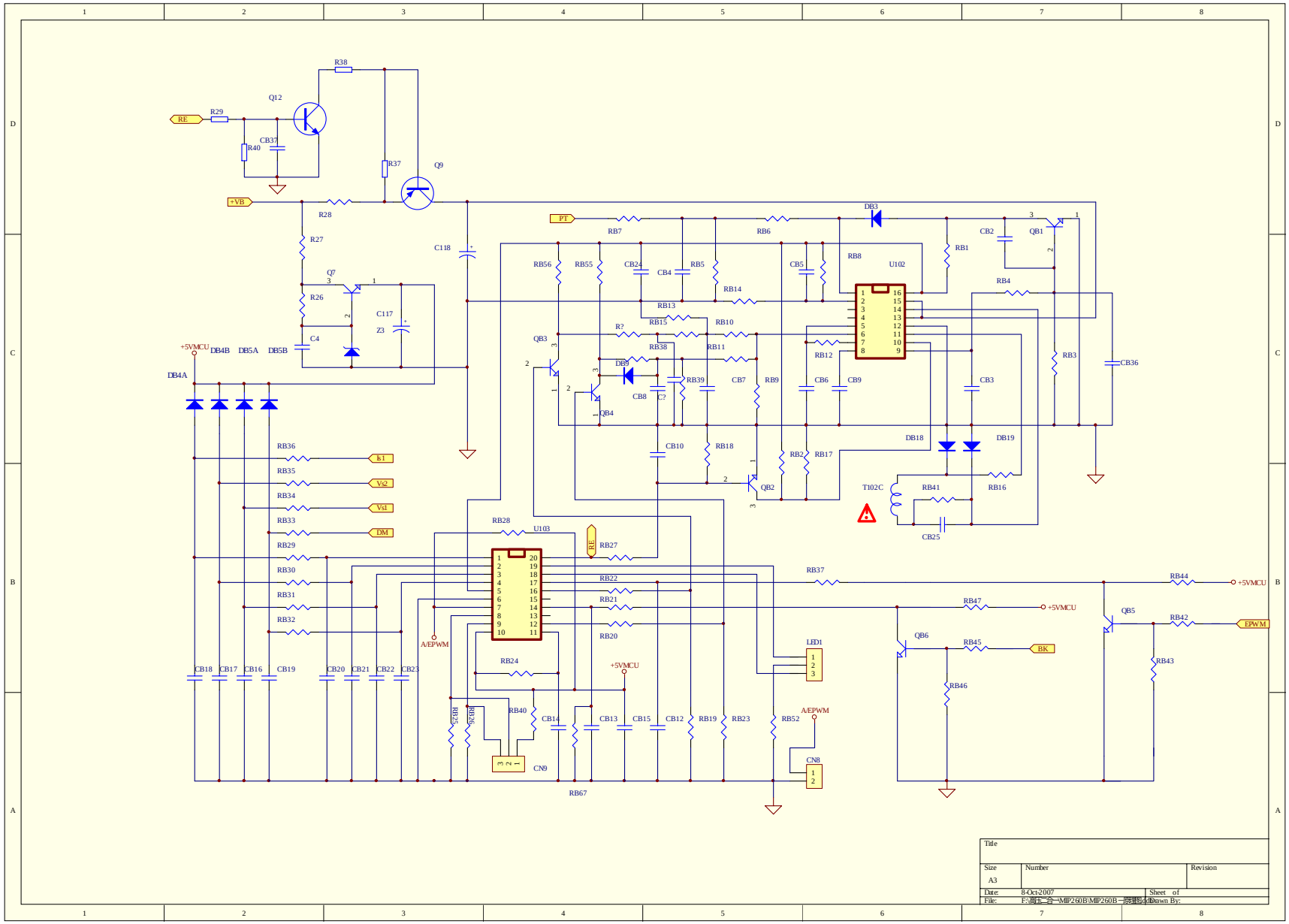
1) PFC



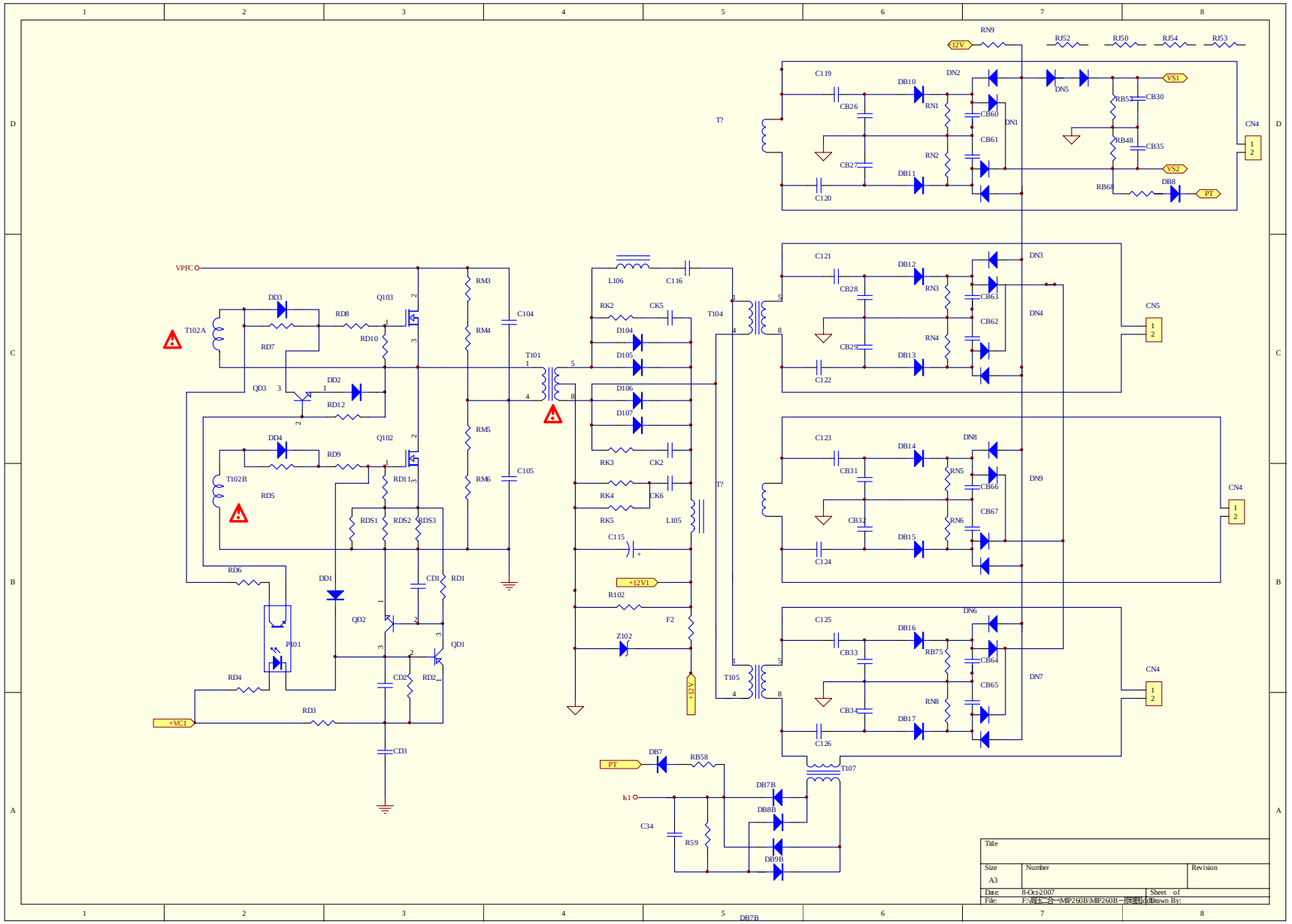
2) 5VSTB


+HV1
RV1
RV2
QV1
RV3
QV2
CV1
RV4
QV3
D1
+VCC
C25
C2
D109
R7
T103D
VPFC
R101
D102
C108
T103A
T103B
RK1
CK1
D103
D13
C109
C110
Z101
L104
C113
+12V1
R22
Z4
Q8
CK7
C3
+5V
A
Q104
R1
R2
Q1
R3
R4
R5
+VC1
U2
RS1
RS2
RS3
R6
Z9
C107
P103
D3
T103C
CK4
C111
R18
Q3
R14
Z2
+VSB
+5VSB
R25
R9
R10
CK8
U101
R13
R12
R11
C1
Z5
Z1
Q2
+VCC
R8
+VC
P102
R24
C5
R23
R21
SB
R16
Q4
Q6
Q5
R30
C6
R31
R29
R35
R34
R33
Q10
Q11
R36
Title
Size
A3
Number
Revision
Date:
8-Oct-2007
Sheet of
File:
F:\周士会--MIP260B\MIP260B一级电路.ddb
Drawn By:

3) INVERTER


R38
Q12
RE
R29
CB37
R40
R37
Q9
+VB
R28
R27
C118
Q7
R26
C117
Z3
C4
+5VMCU
DB4B
DB5A
DB5B
DB4A
PT
RB7
RB6
DB3
CB2
QB1
RB8
U102
RB1
RB4
RB56
RB55
CB24
CB4
RB5
CB5
RB14
RB13
RB15
RB10
R?
RB38
RB11
RB12
RB3
CB36
QB3
DB9
CB8
C?
RB39
CB7
RB9
CB6
CB9
CB3
QB4
CB10
RB18
DB18
DB19
RB2
RB17
QB2
T102C
RB41
RB16
CB25
RB36
RB35
RB34
RB33
RB29
RB30
RB31
RB32
ks1
Vs2
Vs1
DM
RB28
U103
RE
RB27
RB37
RB22
RB21
RB20
RB44
+5VMCU
RB47
+5VMCU
QB5
RB42
EPWM
QB6
RB45
BK
RB43
RB46
A/EPWM
CB18
CB17
CB16
CB19
CB20
CB21
CB22
CB23
RB24
+5VMCU
LED1
RB40
CB14
CB13
CB15
CB12
RB19
RB23
RB52
A/EPWM
RB35
RB36
CN9
CN8
RB67
Title
Size
A3
Number
Revision
Date:
8-Oct-2007
Sheet of
File:
Drawn By:

4） 12VCC


RN9
12V
RJ52
RJ50
RJ54
RJ53
C119
DB10
DN2
DN5
VS1
CB26
RN1
CB60
DN1
RB52
CB30
T?
CN4
CB61
RB48
CB35
CB27
RN2
VS2
DB11
RB68
DB8
PT
C120
C121
DB12
DN3
CB28
RN3
CB63
DN4
CN5
CB62
CB29
RN4
DB13
C122
C123
DB14
DN8
CB31
RN5
CB66
DN9
CB67
CB32
RN6
DB15
C124
C125
DB16
DN6
CB33
RB75
CB64
DN7
CB65
CB34
RN8
DB17
C126
T107
VPFC
T102A
DD3
Q103
RD8
RD10
RD7
RM3
RM4
C104
T101
DD2
QD3
RD12
DD4
Q102
RD9
RD11
T102B
RD5
RM5
RM6
C105
RDS1
RDS2
RDS3
RD6
DD1
CD1
RD1
QD2
P101
QD1
RD4
CD2
RD2
RD3
+VC1
CD3
L106
C116
RK2
CK5
T104
D104
D105
D106
D107
RK3
CK2
RK4
CK6
RK5
L105
C115
+12V1
R102
F2
Z102
+12V
T105
PT
DB7
RB58
Is1
C34
R59
DB7B
DB8B
DB9B
Title
Size
A3
Number
Revision
Date:
8-Oct-2007
Sheet of
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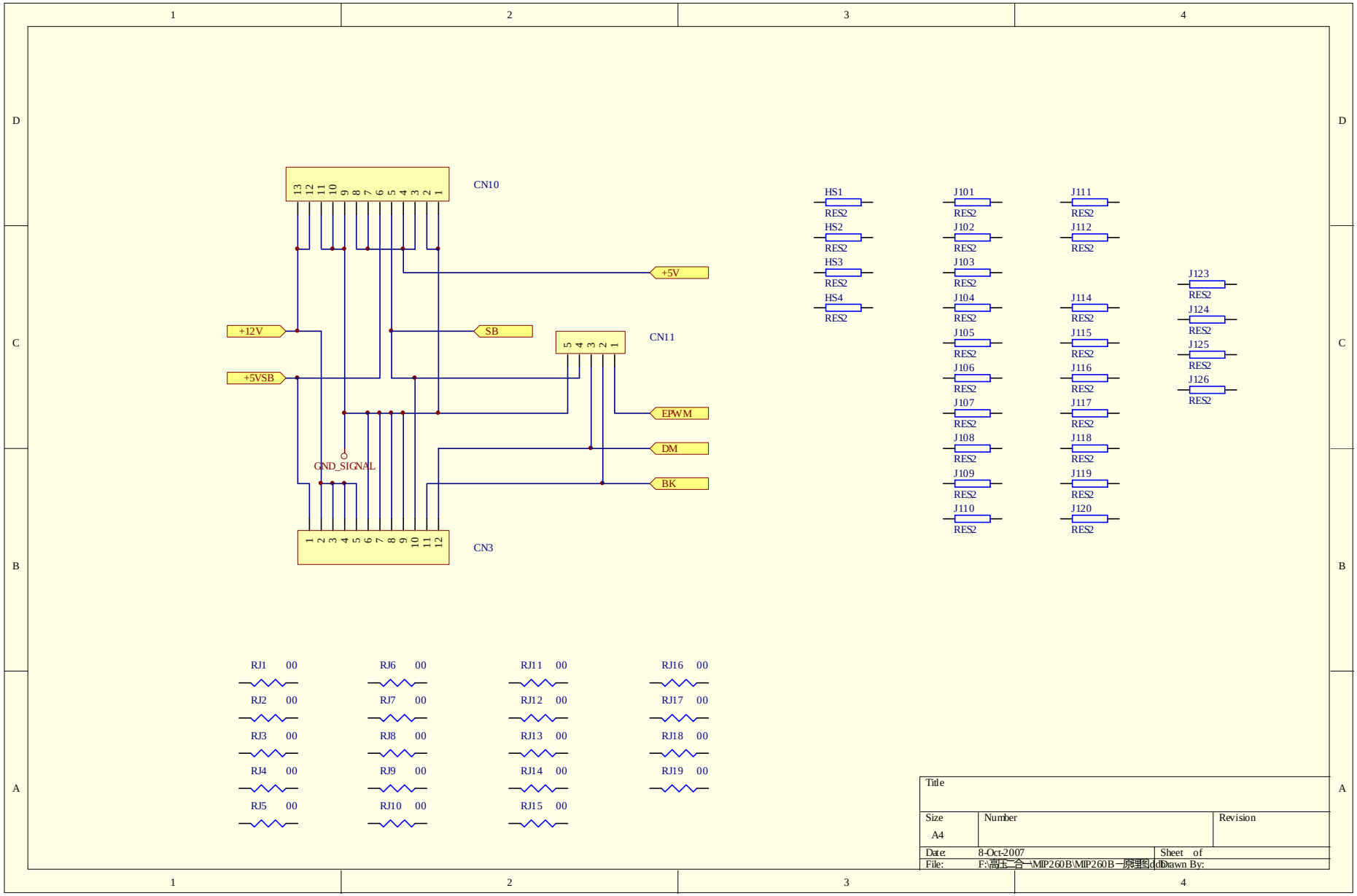
Drawn By:

5) OUT


CN10
13 12 11 10 9 8 7 6 5 4 3 2 1
+5V
+12V
SB
+5VSB
CN11
5 4 3 2 1
EPWM
DM
BK
GND_SIGNAL
1 2 3 4 5 6 7 8 9 10 11 12
CN3
HS1 RES2
HS2 RES2
HS3 RES2
HS4 RES2
J101 RES2
J102 RES2
J103 RES2
J104 RES2
J105 RES2
J106 RES2
J107 RES2
J108 RES2
J109 RES2
J110 RES2
J111 RES2
J112 RES2
J114 RES2
J115 RES2
J116 RES2
J117 RES2
J118 RES2
J119 RES2
J120 RES2
J123 RES2
J124 RES2
J125 RES2
J126 RES2
RJ1 00
RJ2 00
RJ3 00
RJ4 00
RJ5 00
RJ6 00
RJ7 00
RJ8 00
RJ9 00
RJ10 00
RJ11 00
RJ12 00
RJ13 00
RJ14 00
RJ15 00
RJ16 00
RJ17 00
RJ18 00
RJ19 00
Title
Size A4
Number
Revision
Date: 8-Oct-2007
Sheet of
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Drawn By:

2. MIP320G-A(LCD32P08A)

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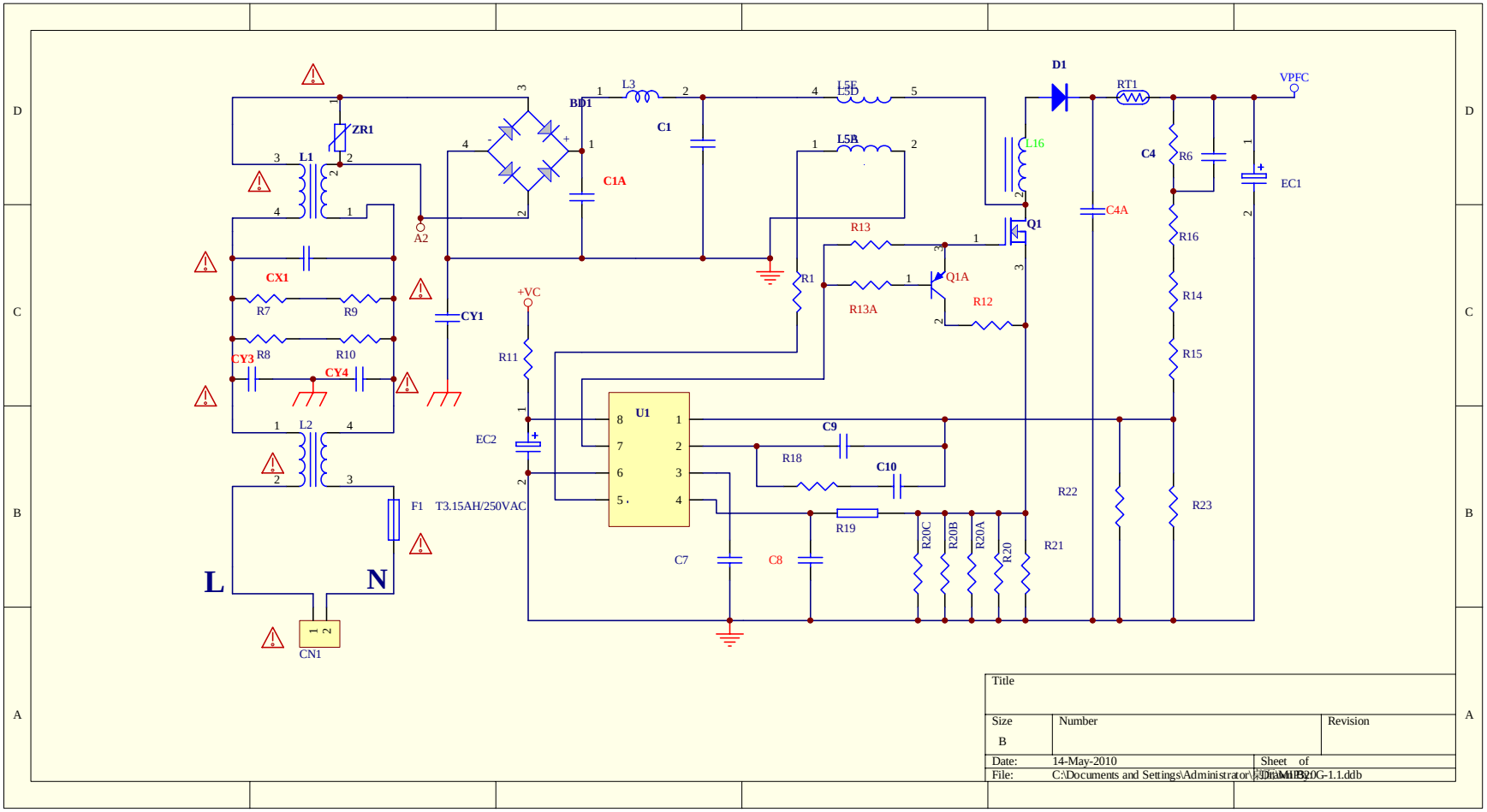
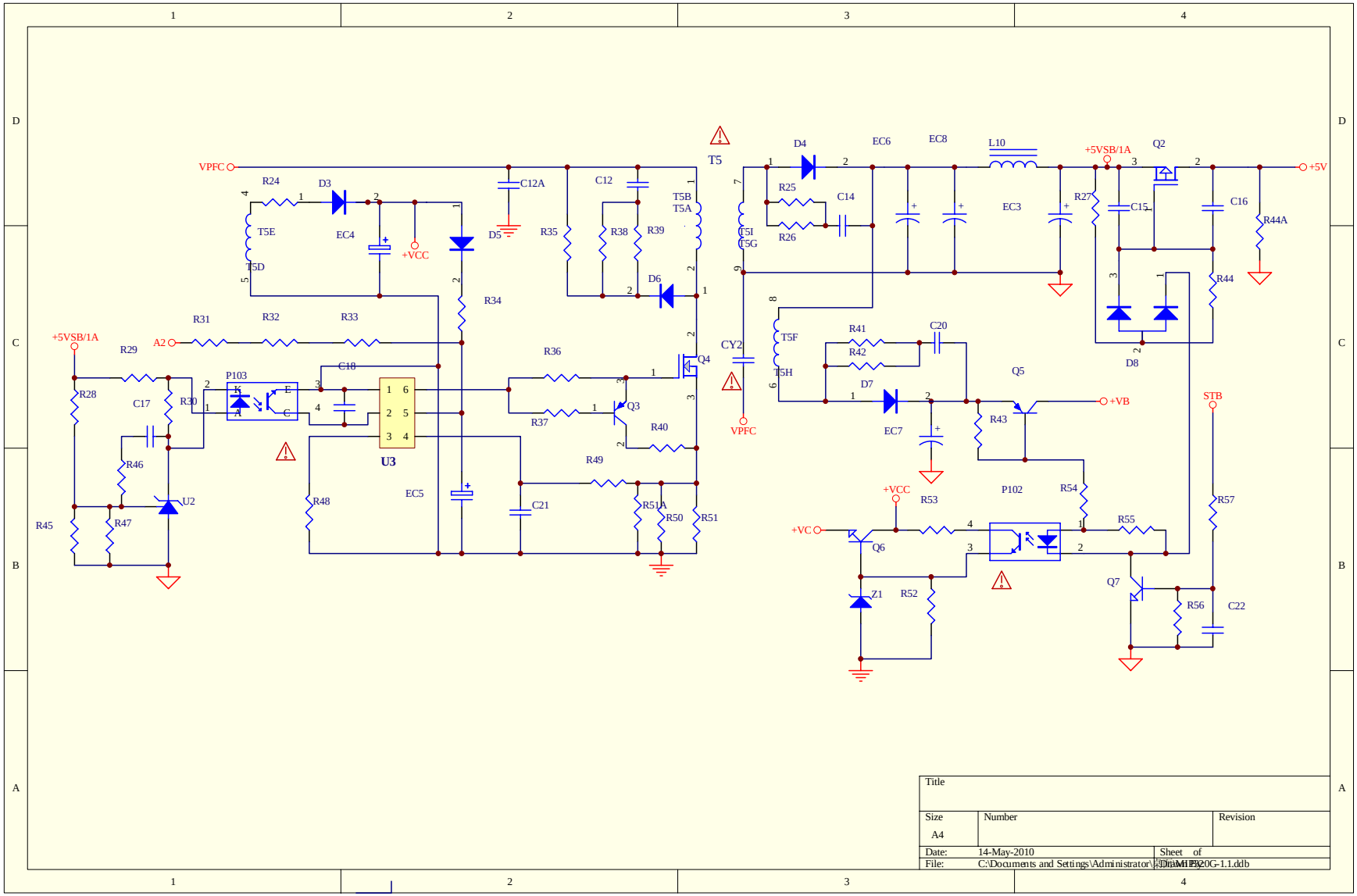


2） 5VSTB


VPFC
R24
D3
T5E
T5D
EC4
+VCC
C12A
D5
C12
T5B
T5A
R35
R38
R39
D6
R34
R31
R32
R33
+5VSB/1A
A2
R29
R28
C17
R30
P103
C18
U3
R46
U2
R45
R47
R48
EC5
C21
R49
R36
Q4
Q3
R37
R40
R51A
R50
R51
T5
D4
EC6
EC8
L10
+5VSB/1A
Q2
+5V
R25
C14
R26
T5I
T5G
EC3
R27
C15
C16
R44A
R44
D8
CY2
T5F
T5H
R41
R42
C20
D7
Q5
+VB
EC7
R43
STB
VPFC
+VCC
R53
P102
R54
R55
R57
+VC
Q6
Z1
R52
Q7
R56
C22
Title
Size
A4
Number
Revision
Date:
14-May-2010
Sheet of
File:
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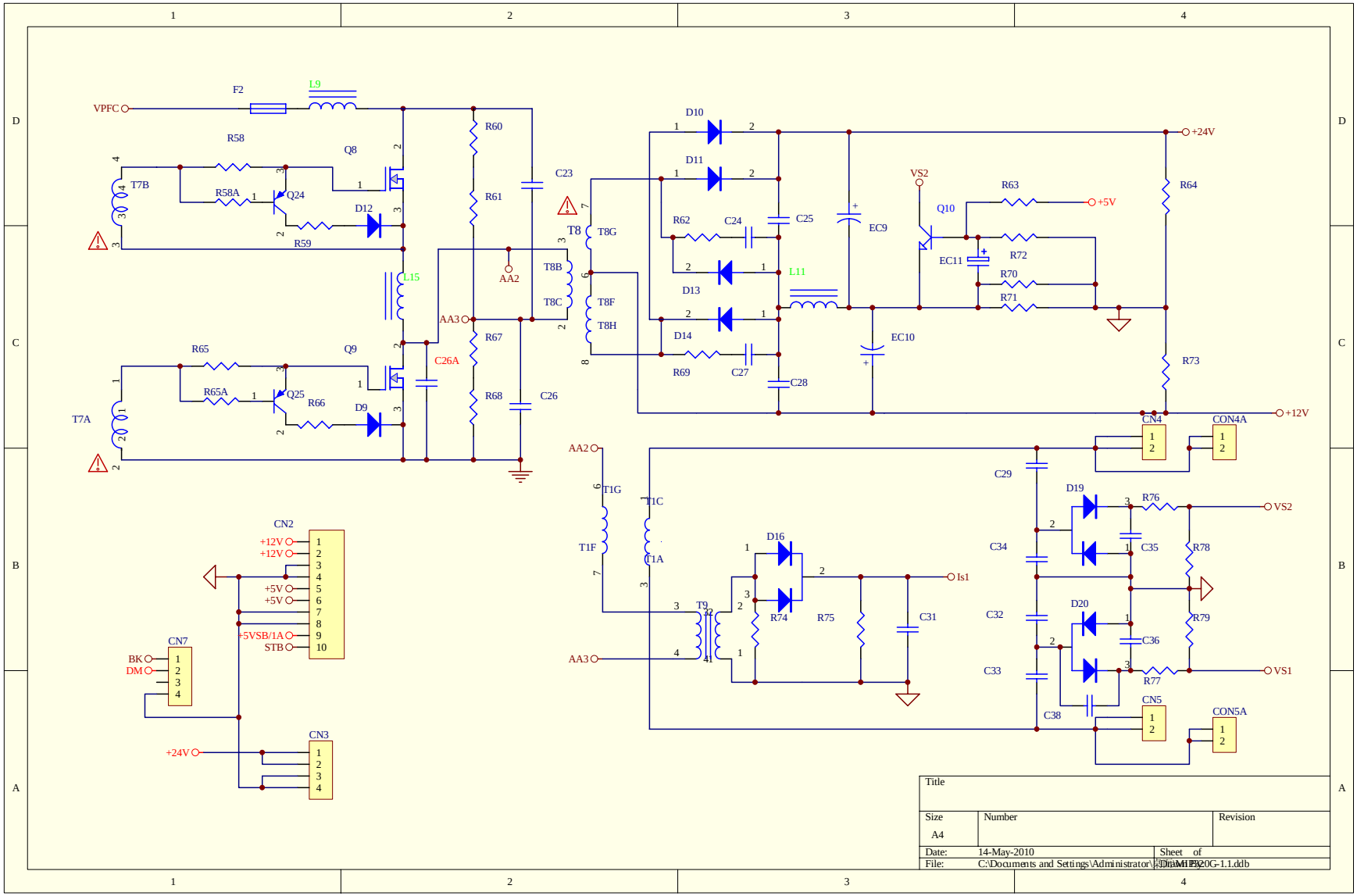
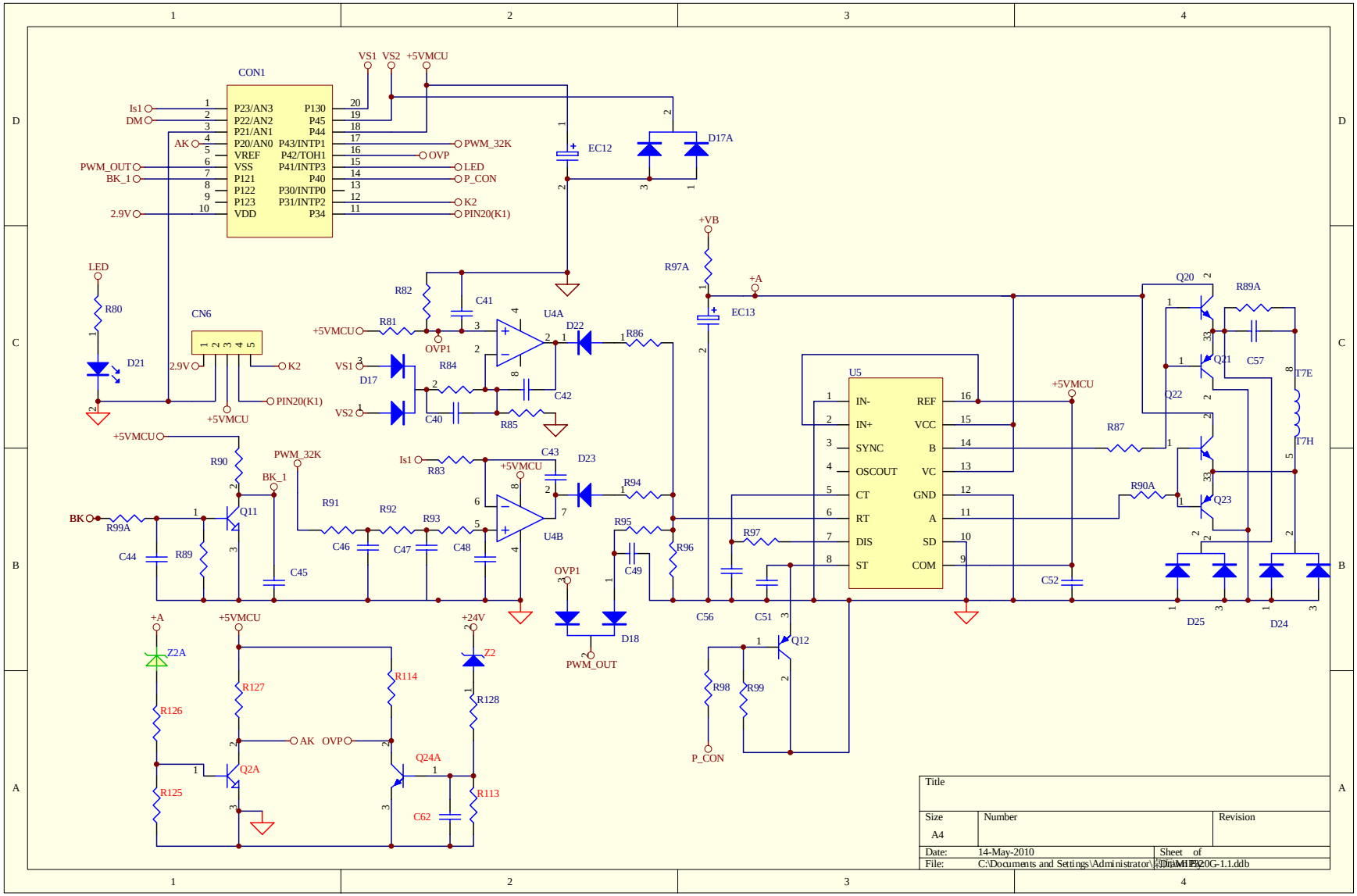
3）12VCC


VPFC
F2
L9
R58
Q8
T7B
R58A
Q24
D12
R59
R60
R61
C23
L15
AA2
AA3
R65
Q9
T7A
R65A
Q25
R66
D9
C26A
R67
R68
C26
T8
T8G
T8B
T8C
T8F
T8H
D10
D11
D13
D14
R62
C24
C25
R69
C27
C28
L11
EC9
EC10
VS2
Q10
R63
+5V
EC11
R72
R70
R71
R64
R73
+24V
+12V
CN4
CON4A
C29
D19
R76
VS2
C34
C35
R78
C32
D20
R79
C36
C33
R77
VS1
CN5
CON5A
C38
T1G
T1C
T1F
T1A
T9
D16
R74
R75
C31
Is1
CN2
+12V
+12V
+5V
+5V
+5VSB/1A
STB
CN7
BK
DM
CN3
+24V
Title
Size
A4
Number
Revision
Date:
14-May-2010
Sheet of
File:
C:\Documents and Settings\Administrator\...\PA320G-1.1.ddb

4) INVERTER


CON1
VS1 VS2 +5VMCU
Is1
DM
AK
PWM_OUT
BK_1
2.9V
P23/AN3 P130
P22/AN2 P45
P21/AN1 P44
P20/AN0 P43/INTP1
VREF P42/TOH1
VSS P41/INTP3
P121 P40
P122 P30/INTP0
P123 P31/INTP2
VDD P34
PWM_32K
OVP
LED
P_CON
K2
PIN20(K1)
EC12
D17A
+VB
R97A
+A
EC13
LED
R80
D21
CN6
2.9V
K2
PIN20(K1)
+5VMCU
R82
C41
R81
OVP1
U4A
D22
R86
VS1
D17
R84
VS2
C40
C42
R85
U5
IN- REF
IN+ VCC
SYNC B
OSCOUT VC
CT GND
RT A
DIS SD
ST COM
Q20
R89A
Q21
C57
T7E
Q22
T7H
R87
Q23
R90A
D25
D24
C52
R90
PWM_32K
BK_1
BK
R99A
Q11
C44
R89
C45
R91
R92
R93
C46
C47
C48
U4B
C43
D23
R94
R95
R96
C49
OVP1
D18
PWM_OUT
C56
C51
R97
Q12
R98
R99
P_CON
+24V
Z2A
Z2
R126
R127
R114
R128
AK OVP
Q2A
Q24A
R125
R113
C62
Title
Size A4
Number
Revision
Date: 14-May-2010
Sheet of
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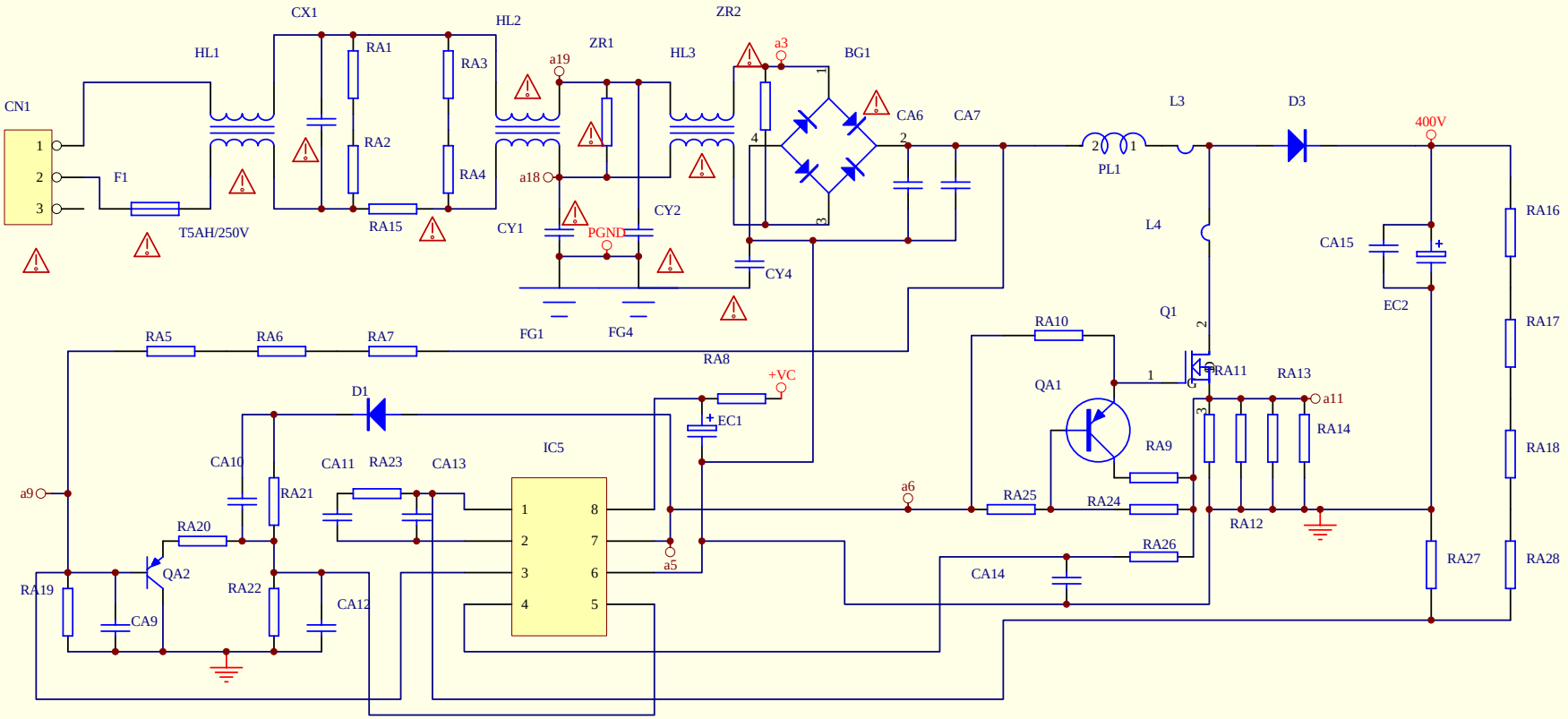
3. MIP328B-K-1(LCD37P08)

1） PFC



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Size A4	Number	Revision
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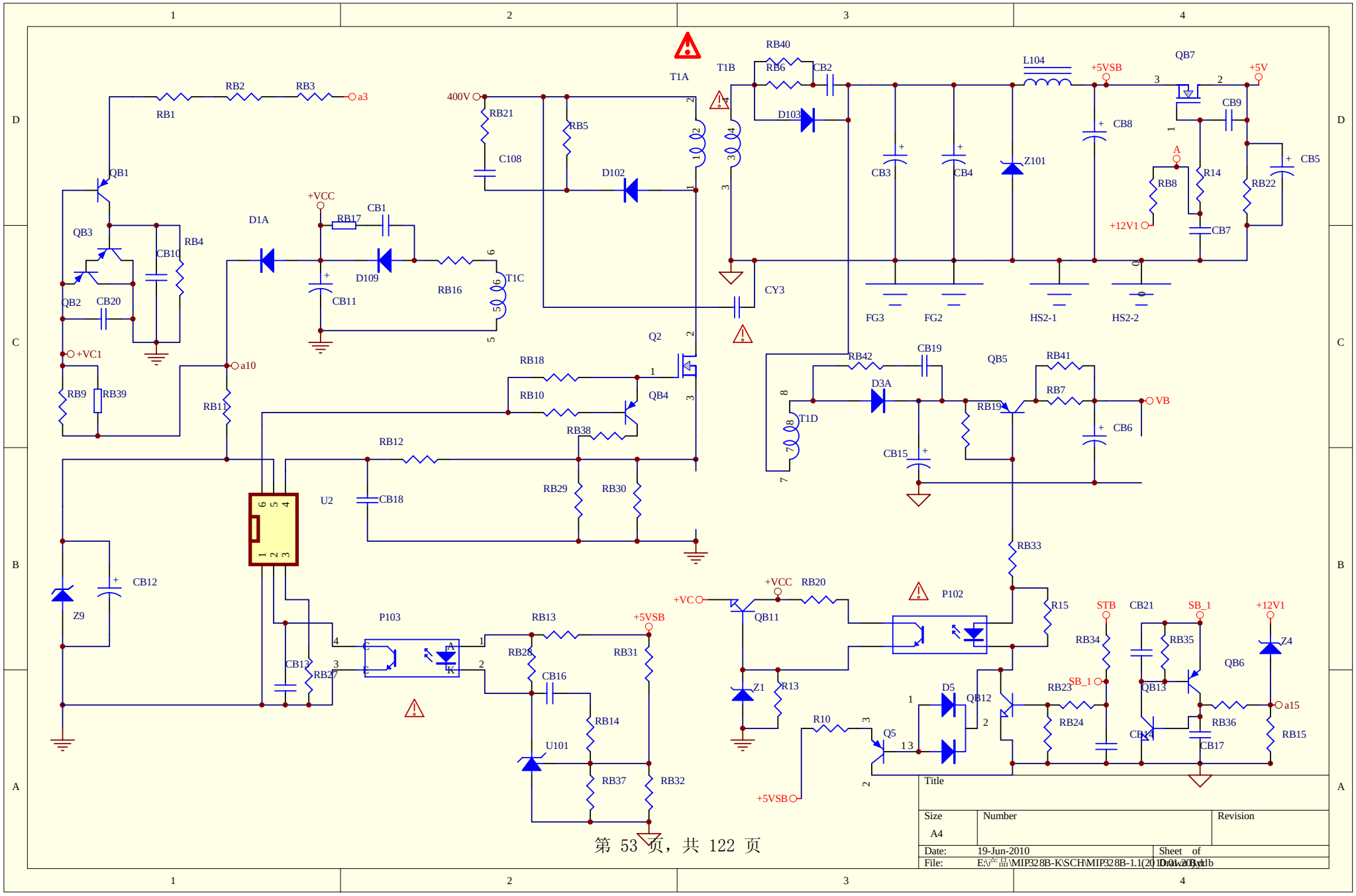
2) 5VSTB


RB1
RB2
RB3
a3
400V
RB21
C108
RB5
D102
T1A
T1B
RB40
RB6
CB2
D103
L104
+5VSB
QB7
+5V
CB9
CB8
CB3
CB4
Z101
A
RB8
R14
RB22
CB5
+12V1
CB7
FG3
FG2
HS2-1
HS2-2
CY3
QB1
QB3
RB4
CB10
QB2
CB20
+VC1
D1A
+VCC
CB1
RB17
D109
CB11
RB16
T1C
a10
RB9
RB39
RB11
Q2
RB18
RB10
QB4
RB38
RB12
U2
CB18
RB29
RB30
RB42
CB19
QB5
RB41
D3A
RB19
RB7
VB
T1D
CB15
CB6
RB33
Z9
CB12
P103
CB13
RB27
RB28
RB13
+5VSB
RB31
CB16
RB14
U101
RB37
RB32
+VCC
RB20
QB11
P102
R15
STB
CB21
SB_1
+12V1
RB34
RB35
Z4
QB6
Z1
R13
D5
QB12
SB_1
RB23
QB13
a15
R10
Q5
RB24
RB36
CB14
CB17
RB15
+5VSB
Title
Size
A4
Number
Revision
Date:
19-Jun-2010
Sheet of
File:
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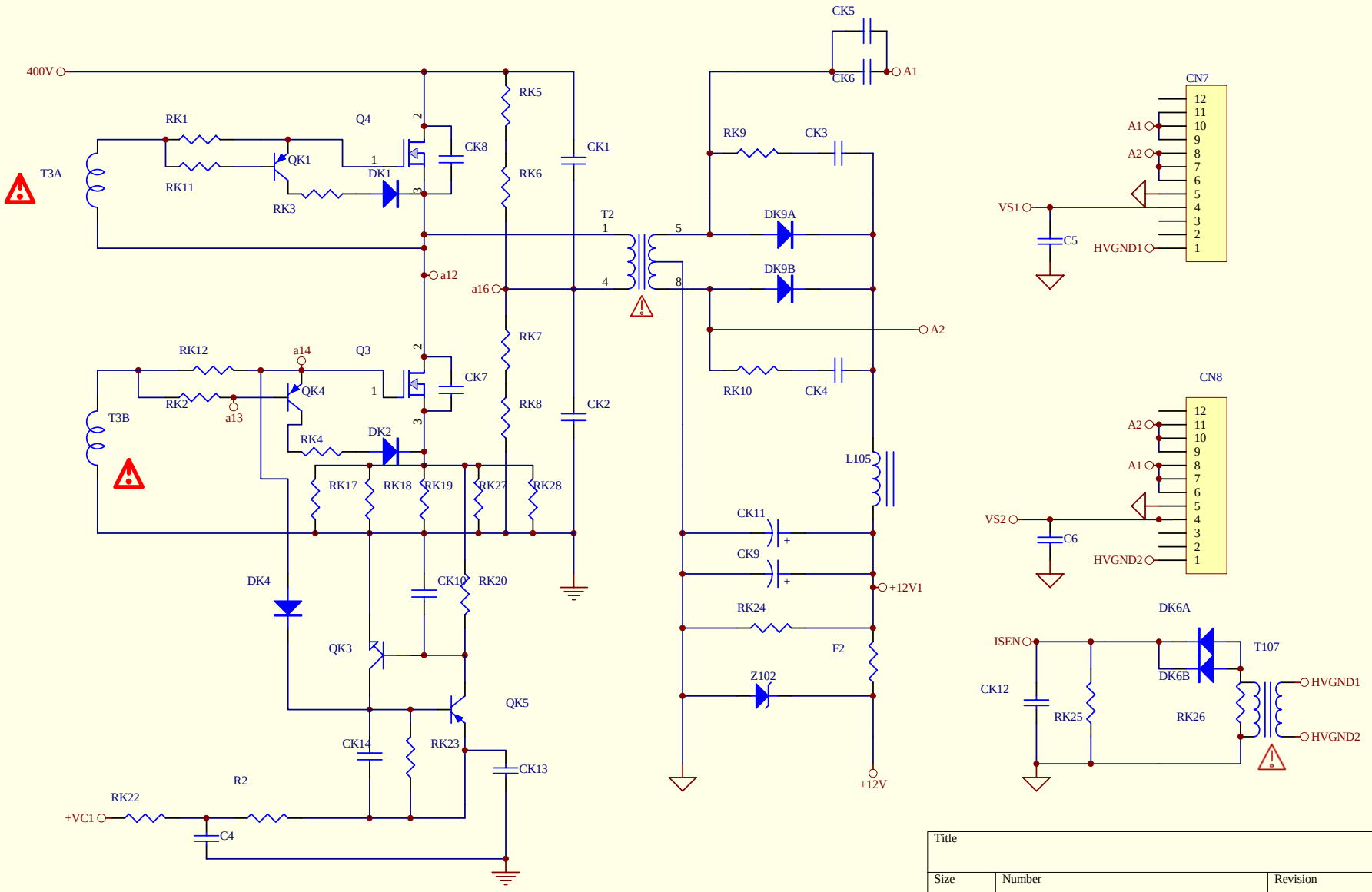
3) INVERTER



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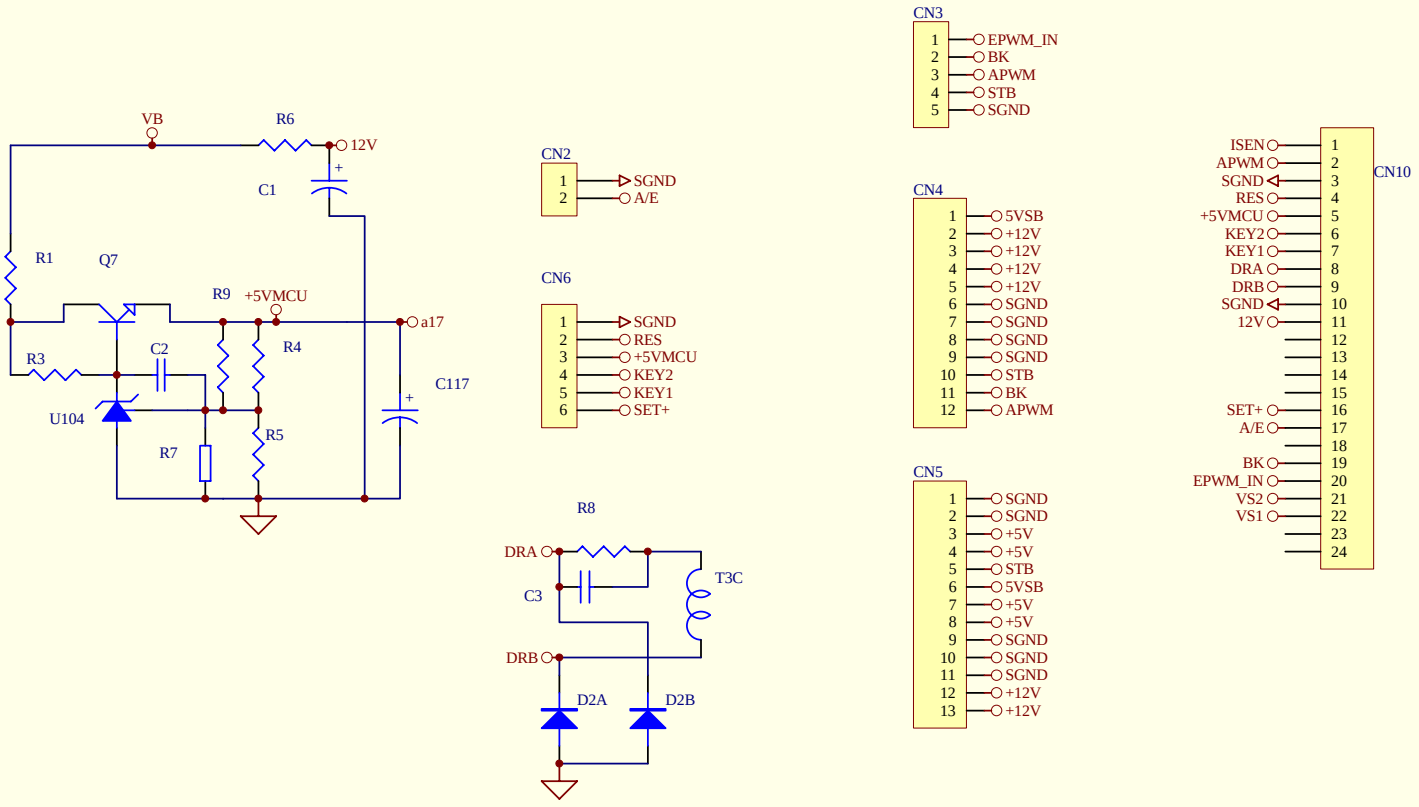

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Size A4	Number	Revision
Date: 19-Jun-2010		Sheet of
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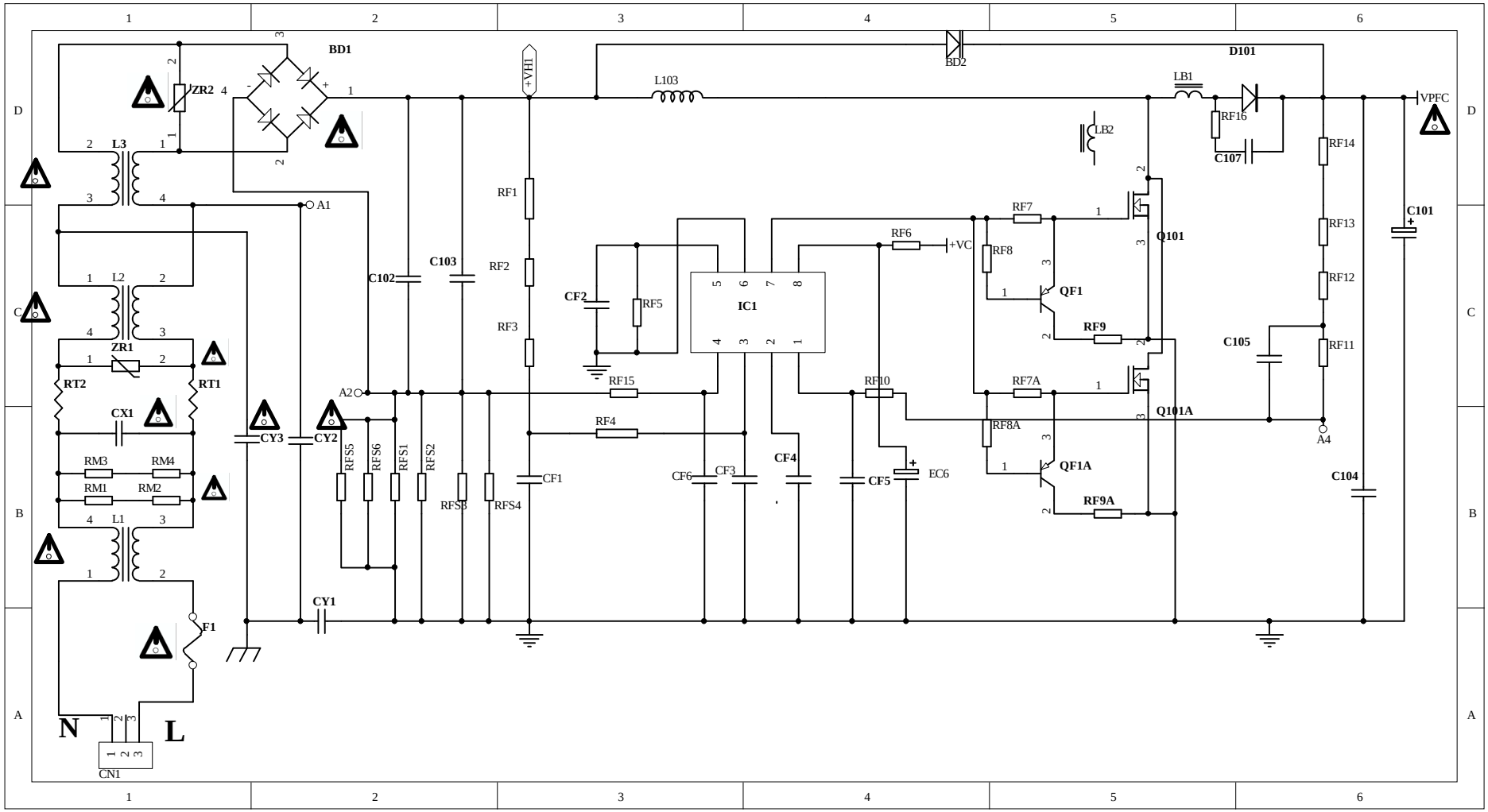
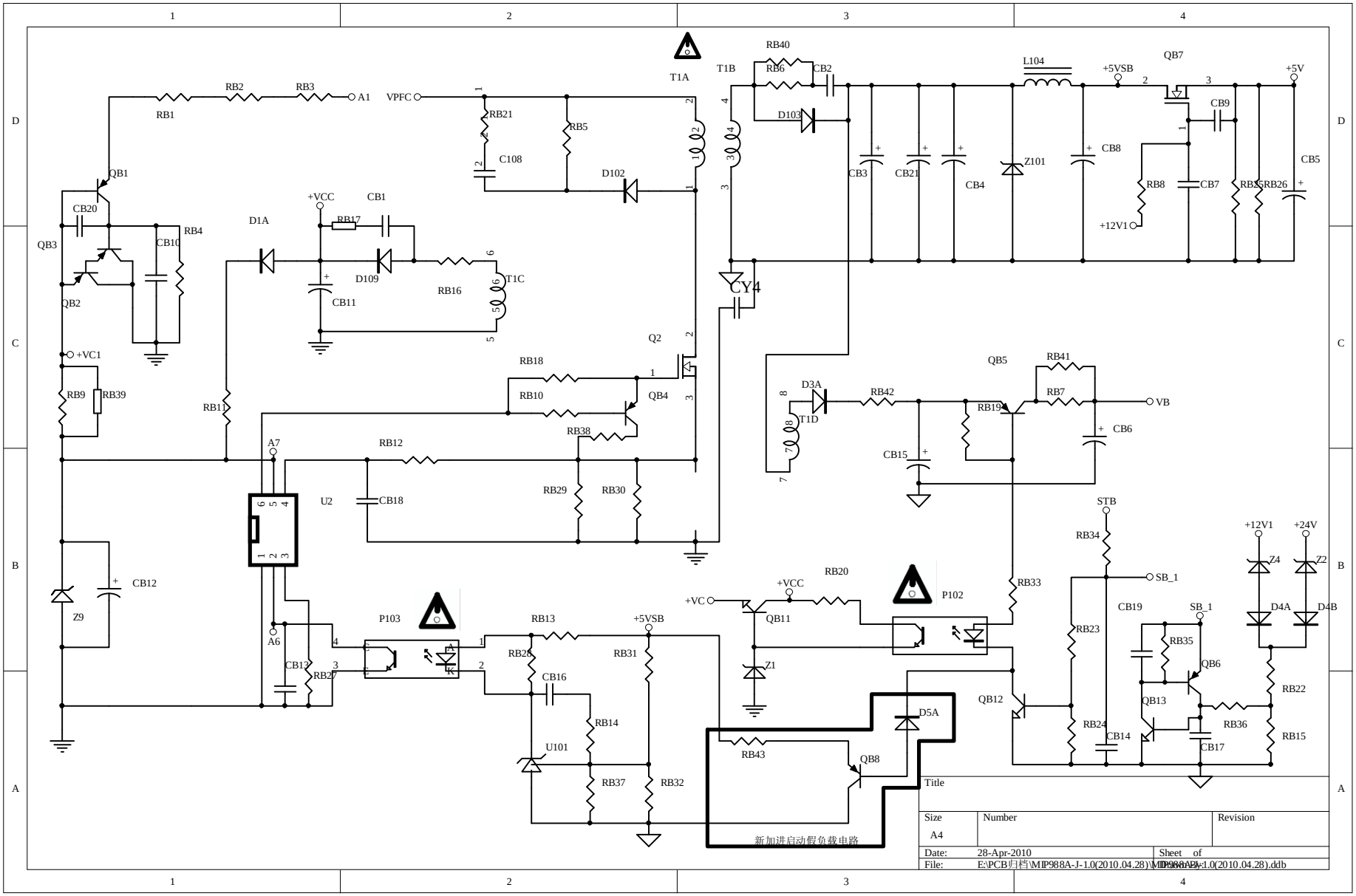
4. MIP988-J(LCD42P08A)

1) PFC



2） 5VSTB


RB40
T1B
RB6
CB2
L104
+5VSB
QB7
+5V
T1A
RB2
RB3
A1
VPFC
RB1
RB21
RB5
D103
CB9
C108
D102
CB3
CB21
CB4
Z101
CB8
CB5
QB1
CB20
+VCC
CB1
D1A
RB17
RB8
CB7
RB3
RB26
+12V1
QB3
RB4
CB10
D109
T1C
RB16
CB11
CY4
QB2
+VC1
Q2
RB18
RB10
QB4
RB38
QB5
RB41
D3A
RB42
RB7
VB
T1D
RB19
CB6
CB15
RB9
RB39
RB11
A7
RB12
U2
CB18
RB29
RB30
STB
RB34
+12V1
+24V
Z4
Z2
SB_1
CB12
Z9
P103
A6
RB20
+VCC
+VC
QB11
P102
RB33
CB19
SB_1
D4A
D4B
RB23
RB35
QB6
RB22
CB13
RB27
RB13
+5VSB
RB28
RB31
CB16
Z1
QB12
QB13
RB36
RB15
D5A
RB14
RB24
CB14
CB17
U101
RB43
QB8
RB37
RB32
新加进启动假负载电路
Title
Size
A4
Number
Revision
Date:
28-Apr-2010
Sheet of
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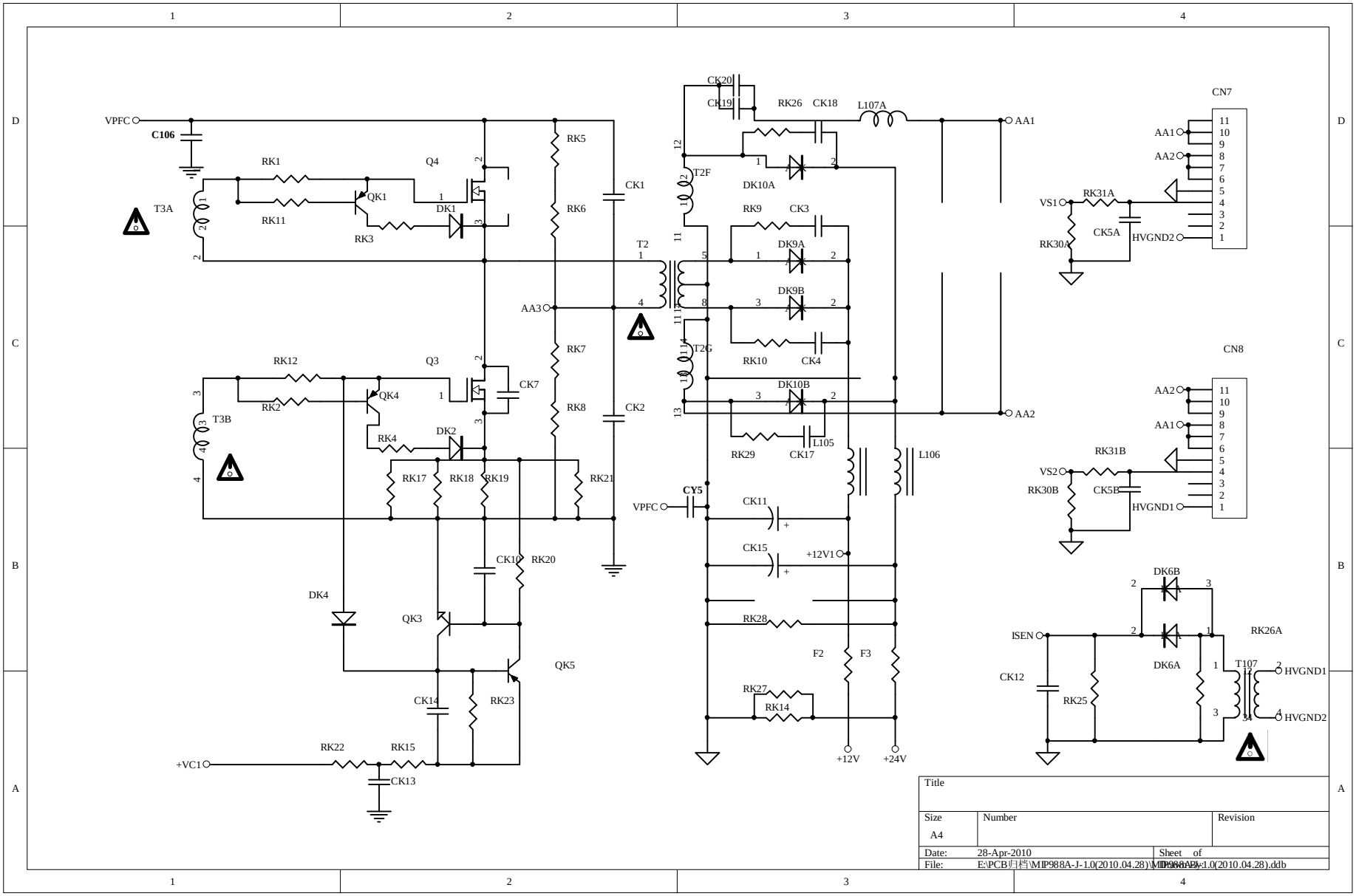
3) INVERTER


VPFC
C106
RK1
Q4
QK1
DK1
RK11
RK3
T3A
RK5
RK6
CK1
T2
AA3
RK7
RK8
CK2
RK12
Q3
QK4
CK7
RK2
T3B
RK4
DK2
RK17
RK18
RK19
RK21
CK10
RK20
DK4
QK3
QK5
CK14
RK23
RK22
RK15
+VC1
CK13
CK20
CK19
RK26
CK18
L107A
AA1
T2F
DK10A
RK9
CK3
DK9A
DK9B
T2G
RK10
CK4
DK10B
AA2
RK29
CK17
L105
L106
CY5
CK11
CK15
+12V1
RK28
F2
F3
RK27
RK14
+12V
+24V
CN7
VS1
RK31A
CK5A
RK30A
HVGND2
CN8
VS2
RK31B
RK30B
CK5B
HVGND1
DK6B
DK6A
ISEN
RK26A
CK12
RK25
T107
HVGND1
HVGND2
Title
Size
A4
Number
Revision
Date:
28-Apr-2010
Sheet of
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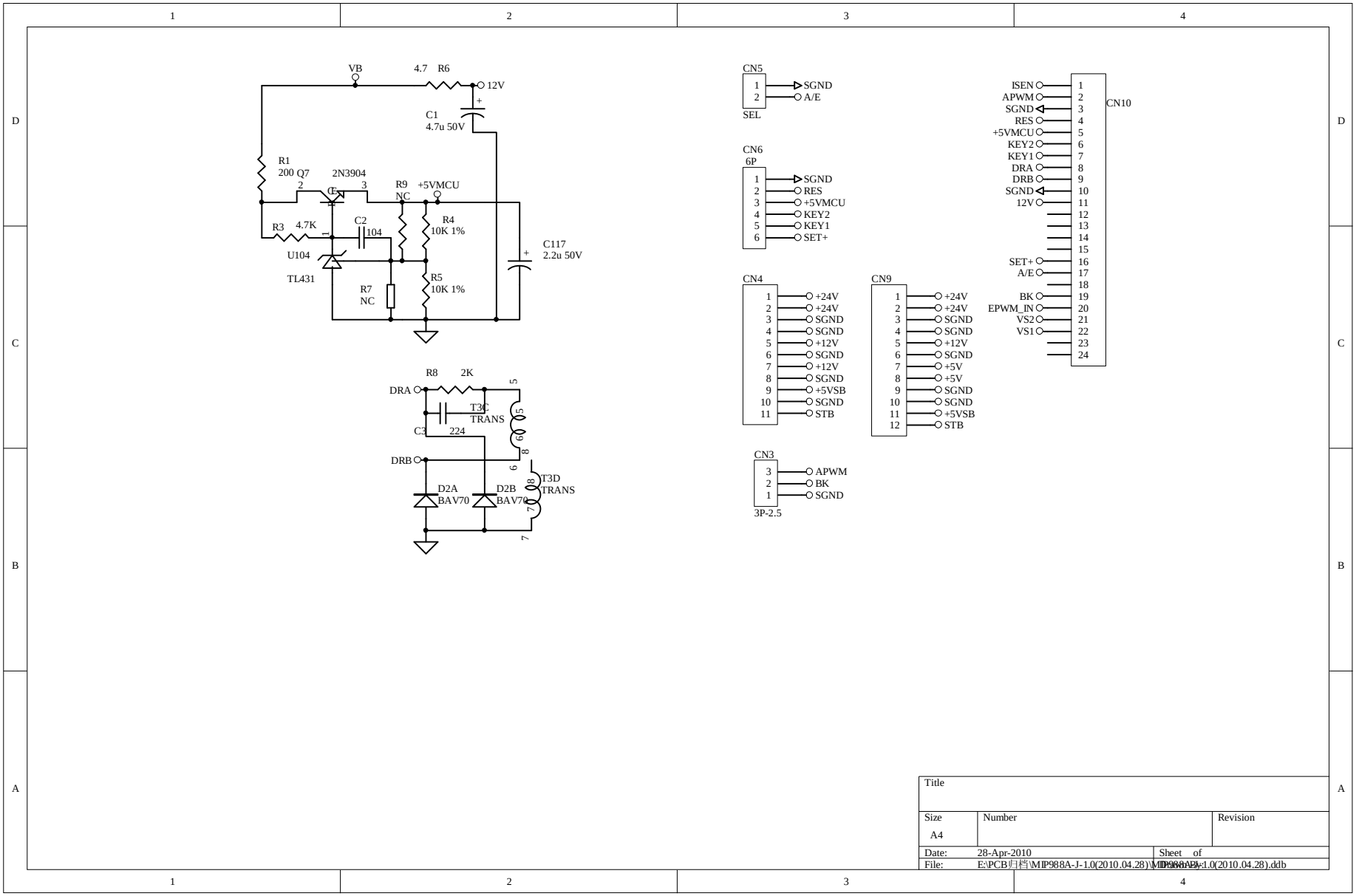
4) OUTPUT


VB
4.7 R6
12V
C1
4.7u 50V
R1
200 Q7
2N3904
R9
NC
+5VMCU
R3 4.7K
C2
104
R4
10K 1%
U104
TL431
R5
10K 1%
R7
NC
C117
2.2u 50V
R8 2K
DRA
T3C
TRANS
C3 224
DRB
D2A
BAV70
D2B
BAV70
T3D
TRANS
CN5
SEL
SGND
A/E
CN6
6P
SGND
RES
+5VMCU
KEY2
KEY1
SET+
CN4
+24V
+24V
SGND
SGND
+12V
SGND
+12V
SGND
+5VSB
SGND
STB
CN9
+24V
+24V
SGND
SGND
+12V
SGND
+5V
+5V
SGND
SGND
+5VSB
STB
CN3
APWM
BK
SGND
3P-2.5
CN10
ISEN
APWM
SGND
RES
+5VMCU
KEY2
KEY1
DRA
DRB
SGND
12V
SET+
A/E
BK
EPWM_IN
VS2
VS1
Title
Size
A4
Number
Revision
Date: 28-Apr-2010
Sheet of
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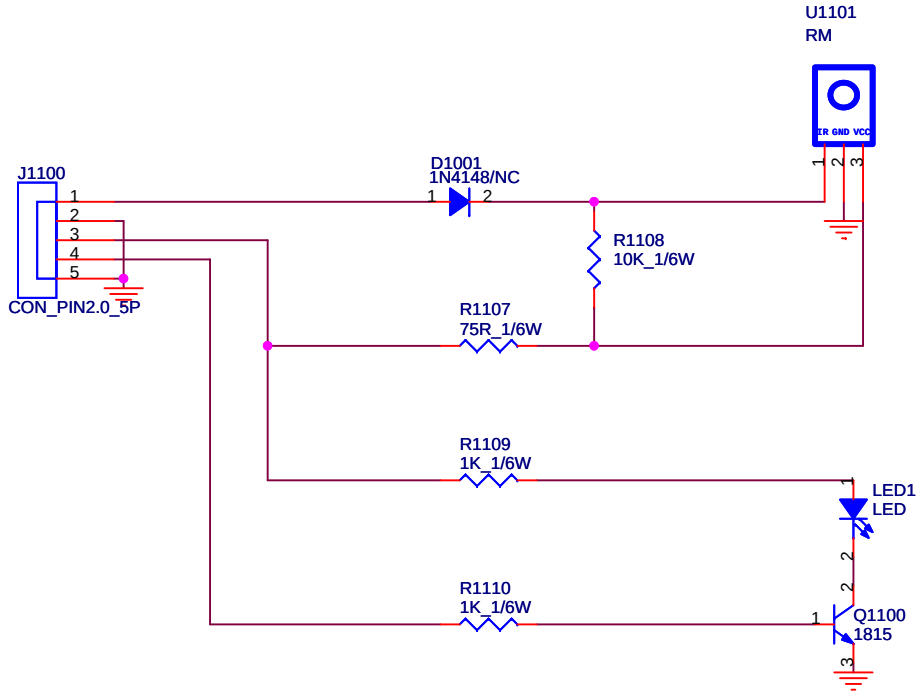
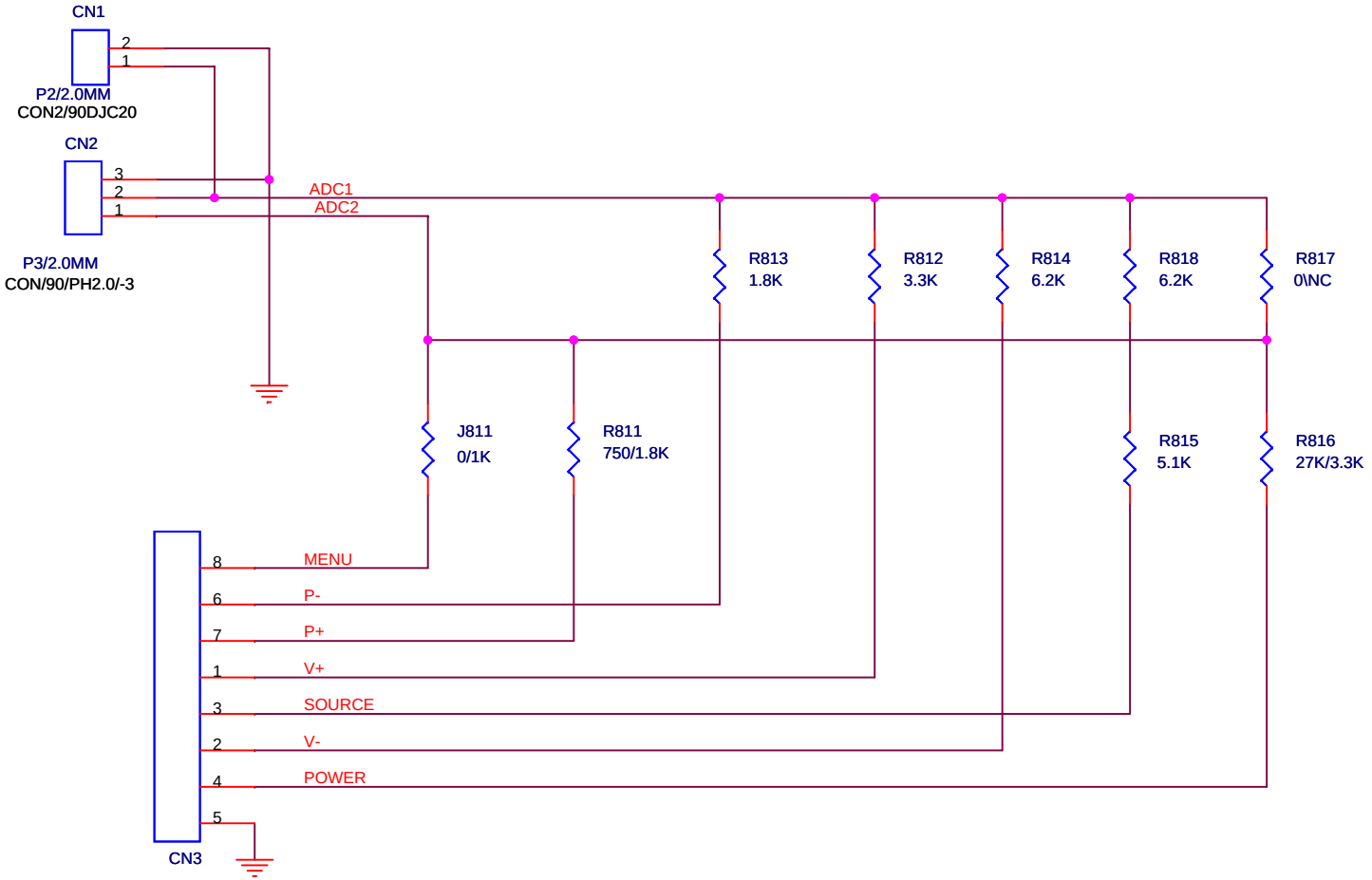
7.3 IR 板



JPE	JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z	
	Title: IR	
	Size: A4 / Document Number: IR_Board	Rev: <01>
	Date: Tuesday, July 20, 2010 / Sheet 1 of 1	

7.4 按键板



JPE	JINPIN ELECTRICAL COMPANY LTD.ZHUHAI.S.E.Z	
	Title: key conversion	
	Size: A4 / Document Number: <Doc>	Rev: <01>
	Date: Friday, July 23, 2010 / Sheet 1 of 1	

MSTAR TSUMV36KU (SD) 主要芯片说明规格

FEATURES

- NTSC/PAL/SECAM Video Decoder
  - Supports NTSC M, NTSC-J, NTSC-4.43, PAL (B,D,G,H,M,N,I,Nc), and SECAM
  - Automatic TV standard detection
  - 2D NTSC and PAL comb-filter for Y/C separation
  - 4 configurable CVBS & Y/C S-video inputs
  - Supports Closed-caption, and V-chip
  - CVBS video output
- Video IF for Multi-Standard Analog TV
  - Digital low IF architecture
  - Stepped-gain PGA with 26 dB tuning range and 1 dB tuning resolution
  - Maximum IF analog gain of 37dB in addition to digital gain
  - Programmable TOP to accommodate different tuner gain to optimize noise and linearity performance
- Multi-Standard TV Sound Decoding/Processing
  - Supports BTSC/A2/EIA-J demodulation and decoding
  - FM stereo & SAP demodulation
  - Audio processing for loudspeaker channel, including volume, balance, mute, tone, and P/G EQ
  - Mstar surround sound effect
- Digital Audio Interface
  - HDMI audio channel processing capability
  - Audio Line-In L/R x3
  - Audio Line-Out L/R x2
  - Built-in audio DAC
  - Built-in audio ADC
  - SIF audio input
- Analog RGB Compliant Input Ports
  - Two analog ports support up to UXGA
  - Supports HDTV RGB/YPbPr/YCbCr
  - Supports Composite Sync and SOG (Sync-on-Green) separator
  - Automatic color calibration
- DVI/HDCP/HDMI Compliant Input Port
  - One DVI/HDMI input port
  - Supports TMDS clock up to 225MHz @ 1080P 60Hz
  - Single link on-chip DVI 1.0 compliant receiver
  - High-bandwidth Digital Content Protection (HDCP) 1.1 compliant receiver
  - High Definition Multimedia Interface (HDMI) 1.3 compliant receiver with CEC support
  - Long-cable tolerant robust receiving
  - Support HDTV up to 1080P
- Auto-Configuration/Auto-Detection
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain, and jitter detection
  - Sync detection for H/V Sync
- High-Performance Scaling Engines
  - Fully programmable shrink/zoom capabilities
  - Nonlinear video scaling supports various modes including Panorama
- Video Processing & Conversion
  - 3-D motion adaptive video de-interlacer
  - Automatic 3:2 pull-down & 2:2 pull-down detection and recovery
  - Edge-oriented adaptive algorithm for smooth low-angle edges
  - MStar 3rd Generation Advanced Color Engine (MStarACE-3) automatic picture enhancement gives:
    - Brilliant and fresh color
    - Intensified contrast and details
    - Vivid skin tone
    - Sharp edge
    - Enhanced depth of field perception
    - Accurate and independent color control
  - sRGB compliance allows end-user to experience the same colors as viewed on CRTs and other displays
  - Programmable 10-bit RGB gamma CLUT

- On-Screen OSD Controller
- 128/256 color palette
- 512 1/2/3-bit/pixel fonts
- Supports 2K attribute/code
- Horizontal and vertical stretch of OSD menus
- Pattern generator for production test
- Supports OSD MUX and alpha blending capability
- Supports blinking and scrolling for closed caption applications

■ LVDS Panel Interface
- Supports 8 bit dual link LVDS up to full HD (1920x1080)
- Supports 2 data output formats: Thine & TI data mappings
- Compatible with TIA/EIA
- Dithering with 6/8 bits options
- Reduced swing for LVDS for low EMI
- Supports flexible spread spectrum frequency with 360Hz~11.8MHz and up to 25% modulation

■ Integrated Micro Controller
- Embedded 8032 micro controller
- Configurable PWM's and GPIO's
- Low-speed ADC inputs for system control
- SPI bus for external flash

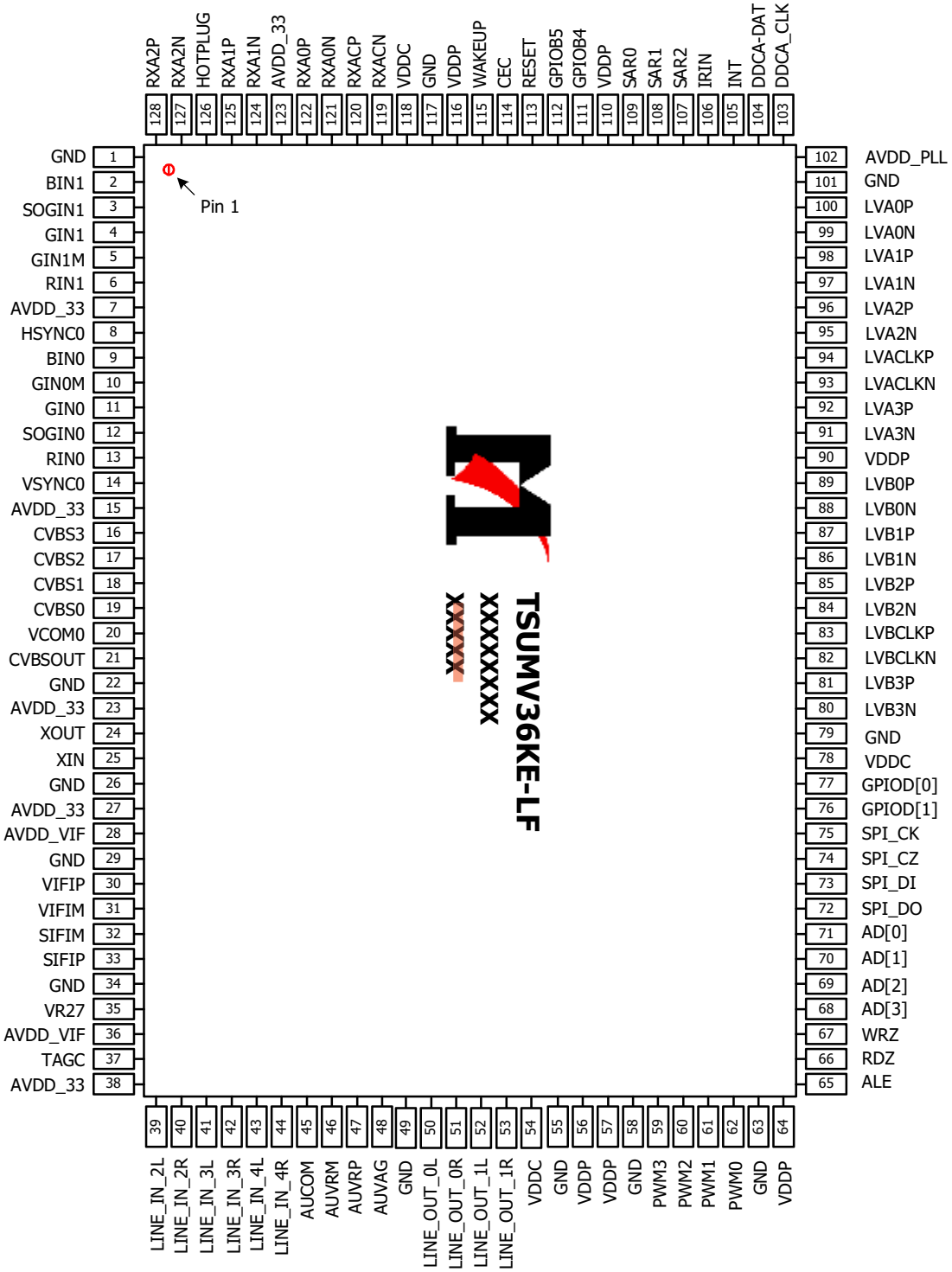
■ Miscellaneous
- 128-pin QFP package
- Integrated power management control with independent power plant to support deep sleep, and wake-up from various input

GENERAL DESCRIPTION

The TSUMV36KU is a high performance and all-in-one IC for multi-function LCD monitor/TV with resolutions up to full HD (1920x1080). It is configured with an integrated triple-ADC/PLL, an integrated DVI/HDCP/HDMI receiver, a multi-standard A/V front-end and baseband decoder, a video de-interlacer, a scaling engine, the MStarACE-3 color engine, an on-screen display controller and a built-in output panel interface. An embedded audio DSP processor gives various of audio manipulation functions for greater audience experiences.

To further reduce system costs, the TSUMV36KU also integrates intelligent power management control capability for green-mode requirements and spread-spectrum support for EMI management.

PIN DIAGRAM (TSUMV36KE)



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. TSUMV36KE comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
TSUMV36KE_pd_v01	• Initial release	Sep 2009

ELECTRICAL SPECIFICATIONS

Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
VIDEO ANALOG INPUT				
Input Voltage Range				
Minimum			0.5	V p-p
Maximum	1.0			V p-p
Input Bias Current			1	uA
Input Full-Scale Matching		1.5		%FS
Brightness Level Adjustment		62		%FS
SWITCHING PERFORMANCE				
Maximum Conversion Rate	165			MSPS
Minimum Conversion Rate			12	MSPS
HSYNC Input Frequency	15		200	kHz
PLL Clock Rate	12		165	MHz
PLL Jitter		500		ps p-p
Sampling Phase Tempco		15		ps/°C
DYNAMIC PERFORMANCE				
Analog Bandwidth, Full Power		250		MHz
DIGITAL INPUTS				
Input Voltage, High (V_{IH})	2.5			V
Input Voltage, Low (V_{IL})			0.8	V
Input Current, High (I_{IH})			-1.0	uA
Input Current, Low (I_{IL})			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High (V_{OH})	VDDP-0.1			V
Output Voltage, Low (V_{OL})			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Buffer Output				
Output Low		1.5		V
Output High		2.0		V

Parameter	Min	Typ	Max	Unit
AUDIO				
ADC Input		2.0		V p-p
DAC Output		2.0		V p-p
SIF Input Range				
Minimum			0.1	V p-p
Maximum	1.0			V p-p
FSSW Input[1]	0		1.8	V
SAR ADC Input	0		3.3	V
FB ADC Input[2]	0		1.25	V

Specifications subject to change without notice.
Notes:
1. **Input full scale is typically 1.8V, but input range is 0 ~ 3.3V.**
2. **Input full scale is 1.25V, but input range is 0 ~ 3.3V.**

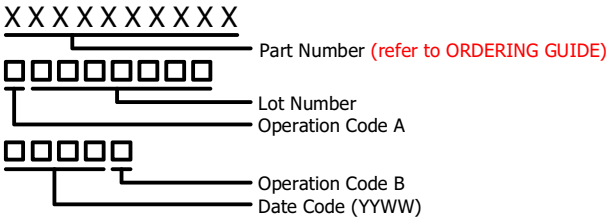
Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
3.3V Supply Voltages	V_{VDD_33}	3.14	3.6	V
1.26V Supply Voltages	V_{VDD_126}	1.2	1.32	V
Input Voltage (5V tolerant inputs)	$V_{IN5Vtol}$		5.0	V
Input Voltage (non 5V tolerant inputs)	V_{IN}		V_{VDD_33}	V
Ambient Operating Temperature	T_A	0	70	°C
Storage Temperature	T_{STG}	-40	150	°C
Junction Temperature	T_J		150	°C

ORDERING GUIDE

Part Number	Temperature Range	Package Description	Package Option
TSUMV36KU-LF	0°C to +70°C	QFP	128

MARKING INFORMATION



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Electrostatic charges accumulate on both test equipment and human body and can discharge without detection. TSUMV36KU comes with ESD protection circuitry; however, the device may be permanently damaged when subjected to high energy discharges. The device should be handled with proper ESD precautions to prevent malfunction and performance degradation.

REVISION HISTORY

Document	Description	Date
TSUMV36KU_ds_v01	• Initial release	Aug 2009
TSUMV36KU_ds_v02	• Revise typos in features	Sep 2009

Features

- **Medium-voltage and Standard-voltage Operation**
  - **5.0 (V_{CC} = 4.5V to 5.5V)**
  - **2.7 (V_{CC} = 2.7V to 5.5V)**
- **Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)**
- **2-wire Serial Interface**
- **Schmitt Trigger, Filtered Inputs for Noise Suppression**
- **Bi-directional Data Transfer Protocol**
- **100 kHz (2.7V) and 400 kHz (5V) Compatibility**
- **Write Protect Pin for Hardware Data Protection**
- **8-byte Page (1K, 2K), 16-byte Page (4K, 8K, 16K) Write Modes**
- **Partial Page Writes are Allowed**
- **Self-timed Write Cycle (10 ms max)**
- **High-reliability**
  - **Endurance: 1 Million Write Cycles**
  - **Data Retention: 100 Years**
- **8-lead PDIP and 8-lead JEDEC SOIC Packages**

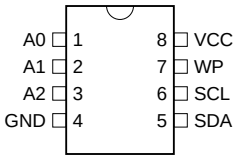
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read-only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many automotive applications where low-power and low-voltage operation are essential. The AT24C01A/02/04/08/16 is available in space-saving 8-lead PDIP and 8-lead JEDEC SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V) and 2.7V (2.7V to 5.5V) versions.

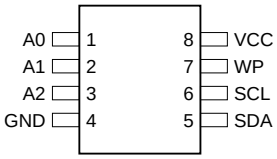
Pin Configurations

Pin Name	Function
A0 - A2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

8-lead PDIP



8-lead SOIC



2-wire Automotive Serial EEPROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

AT24C01A
AT24C02
AT24C04
AT24C08(1)
AT24C16(2)

Note: 1. This device is not recommended for new designs. Please refer to AT24C08A.

2. This device is not recommended for new designs. Please refer to AT24C16A.

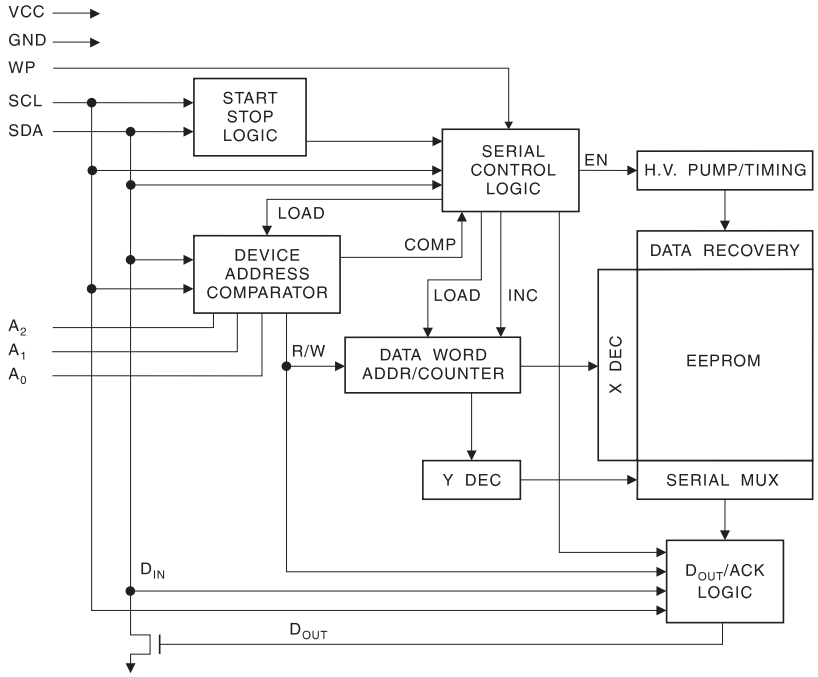
3256D–SEEPR–11/03

Absolute Maximum Ratings

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins, which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

WRITE PROTECT (WP): The AT24C01A/02/04/16 has a Write Protect pin that provides hardware data protection. The Write Protect pin allows normal read/write operations when connected to ground (GND). When the Write Protect pin is connected to V_{CC}, the write protection feature is enabled and operates as shown in the following table.

WP Pin Status	Part of the Array Protected				
	24C01A	24C02	24C04	24C08(1)	24C16(2)
At V_{CC}	Full (1K) Array	Full (2K) Array	Full (4K) Array	Normal Read/ Write Operation	Upper Half (8K) Array
At GND	Normal Read/Write Operations				

Notes: 1. This device is not recommended for new designs. Please refer to AT24C08A.
2. This device is not recommended for new designs. Please refer to AT24C16A.

Memory Organization

AT24C01A, 1K SERIAL EEPROM: Internally organized with 16 pages of 8 bytes each, the 1K requires a 7-bit data word address for random word addressing.

AT24C02, 2K SERIAL EEPROM: Internally organized with 32 pages of 8 bytes each, the 2K requires an 8-bit data word address for random word addressing.

AT24C04, 4K SERIAL EEPROM: Internally organized with 32 pages of 16 bytes each, the 4K requires a 9-bit data word address for random word addressing.

AT24C08, 8K SERIAL EEPROM: Internally organized with 64 pages of 16 bytes each, the 8K requires a 10-bit data word address for random word addressing.

AT24C16, 16K SERIAL EEPROM: Internally organized with 128 pages of 16 bytes each, the 16K requires an 11-bit data word address for random word addressing.

Features

- Single 2.7V - 3.6V Supply
- Serial Peripheral Interface (SPI) Compatible
  - Supports SPI Modes 0 and 3
- 70 MHz Maximum Clock Frequency
- Flexible, Uniform Erase Architecture
  - 4-Kbyte Blocks
  - 32-Kbyte Blocks
  - 64-Kbyte Blocks
  - Full Chip Erase
- Individual Sector Protection with Global Protect/Unprotect Feature
  - One 32-Kbyte Top Boot Sector
  - Two 8-Kbyte Sectors
  - One 16-Kbyte Sector
  - Fifteen 64-Kbyte Sectors
- Hardware Controlled Locking of Protected Sectors
- Flexible Programming Options
  - Byte/Page Program (1 to 256 Bytes)
  - Sequential Program Mode Capability
- Automatic Checking and Reporting of Erase/Program Failures
- JEDEC Standard Manufacturer and Device ID Read Methodology
- Low Power Dissipation
  - 5 mA Active Read Current (Typical)
  - 10 µA Deep Power-down Current (Typical)
- Endurance: 100,000 Program/Erase Cycles
- Data Retention: 20 Years
- Complies with Full Industrial Temperature Range
- Industry Standard Green (Pb/Halide-free/RoHS Compliant) Package Options
  - 8-lead SOIC (150-mil and 200-mil wide)

8-megabit 2.7-volt Only Serial Firmware DataFlash® Memory

AT26DF081A

1. Description

The AT26DF081A is a serial interface Flash memory device designed for use in a wide variety of high-volume consumer-based applications in which program code is shadowed from Flash memory into embedded or external RAM for execution. The flexible erase architecture of the AT26DF081A, with its erase granularity as small as 4 Kbytes, makes it ideal for data storage as well, eliminating the need for additional data storage EEPROM devices.

The physical sectoring and the erase block sizes of the AT26DF081A have been optimized to meet the needs of today's code and data storage applications. By optimizing the size of the physical sectors and erase blocks, the memory space can be used much more efficiently. Because certain code modules and data storage segments must reside by themselves in their own protected sectors, the wasted and unused memory space that occurs with large sectored and large block erase Flash memory devices can be greatly reduced. This increased memory space efficiency allows additional code routines and data storage segments to be added while still maintaining the same overall device density.

3600F–DFLASH–03/07

The AT26DF081A also offers a sophisticated method for protecting individual sectors against erroneous or malicious program and erase operations. By providing the ability to individually protect and unprotect sectors, a system can unprotect a specific sector to modify its contents while keeping the remaining sectors of the memory array securely protected. This is useful in applications where program code is patched or updated on a subroutine or module basis, or in applications where data storage segments need to be modified without running the risk of errant modifications to the program code segments. In addition to individual sector protection capabilities, the AT26DF081A incorporates Global Protect and Global Unprotect features that allow the entire memory array to be either protected or unprotected all at once. This reduces overhead during the manufacturing process since sectors do not have to be unprotected one-by-one prior to initial programming.

Specifically designed for use in 3-volt systems, the AT26DF081A supports read, program, and erase operations with a supply voltage range of 2.7V to 3.6V. No separate voltage is required for programming and erasing.

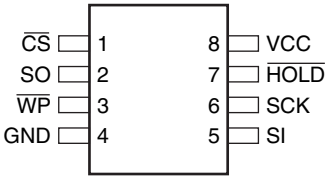
9.3 AT26DF081A

2. Pin Descriptions and Pinouts

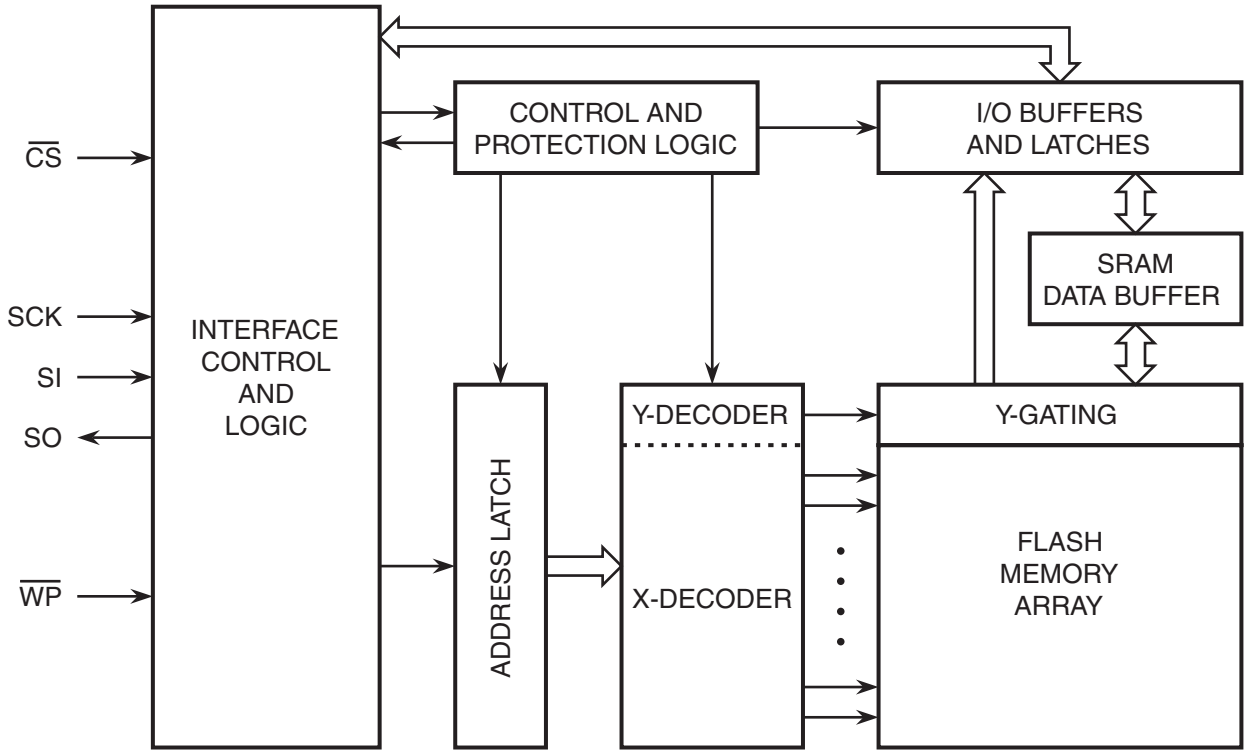
Table 2-1. Pin Descriptions

Symbol	Name and Function	Asserted State	Type
$\overline{CS}$	**CHIP SELECT:** Asserting the $\overline{CS}$ pin selects the device. When the $\overline{CS}$ pin is deasserted, the device will be deselected and normally be placed in standby mode (not Deep Power-down mode), and the SO pin will be in a high-impedance state. When the device is deselected, data will not be accepted on the SI pin. A high-to-low transition on the $\overline{CS}$ pin is required to start an operation, and a low-to-high transition is required to end an operation. When ending an internally self-timed operation such as a program or erase cycle, the device will not enter the standby mode until the completion of the operation.	Low	Input
SCK	**SERIAL CLOCK:** This pin is used to provide a clock to the device and is used to control the flow of data to and from the device. Command, address, and input data present on the SI pin is always latched on the rising edge of SCK, while output data on the SO pin is always clocked out on the falling edge of SCK.		Input
SI	**SERIAL INPUT:** The SI pin is used to shift data into the device. The SI pin is used for all data input including command and address sequences. Data on the SI pin is always latched on the rising edge of SCK.		Input
SO	**SERIAL OUTPUT:** The SO pin is used to shift data out from the device. Data on the SO pin is always clocked out on the falling edge of SCK.		Output
$\overline{WP}$	**WRITE PROTECT:** The $\overline{WP}$ pin controls the hardware locking feature of the device. Please refer to section "Protection Commands and Features" on page 15 for more details on protection features and the $\overline{WP}$ pin. The $\overline{WP}$ pin is internally pulled-high and may be left floating if hardware-controlled protection will not be used. However, it is recommended that the $\overline{WP}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
$\overline{HOLD}$	**HOLD:** The $\overline{HOLD}$ pin is used to temporarily pause serial communication without deselecting or resetting the device. While the $\overline{HOLD}$ pin is asserted, transitions on the SCK pin and data on the SI pin will be ignored, and the SO pin will be in a high-impedance state. The $\overline{CS}$ pin must be asserted, and the SCK pin must be in the low state in order for a Hold condition to start. A Hold condition pauses serial communication only and does not have an effect on internally self-timed operations such as a program or erase cycle. Please refer to section "Hold" on page 30 for additional details on the Hold operation. The $\overline{HOLD}$ pin is internally pulled-high and may be left floating if the Hold function will not be used. However, it is recommended that the $\overline{HOLD}$ pin also be externally connected to V_{CC} whenever possible.	Low	Input
V_{CC}	**DEVICE POWER SUPPLY:** The V_{CC} pin is used to supply the source voltage to the device. Operations at invalid V_{CC} voltages may produce spurious results and should not be attempted.		Power
GND	**GROUND:** The ground reference for the power supply. GND should be connected to the system ground.		Power

Figure 2-1. 8-SOIC Top View



3. Block Diagram



4. Memory Array

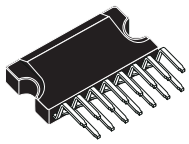
To provide the greatest flexibility, the memory array of the AT26DF081A can be erased in four levels of granularity including a full chip erase. In addition, the array has been divided into physical sectors of various sizes, of which each sector can be individually protected from program and erase operations. The sizes of the physical sectors are optimized for both code and data storage applications, allowing both code and data segments to reside in their own isolated regions. Figure 4-1 on page 5 illustrates the breakdown of each erase level as well as the breakdown of each physical sector.

TDA7266SA

7W+7W DUAL BRIDGE AMPLIFIER

- WIDE SUPPLY VOLTAGE RANGE (3.5-18V)
- MINIMUM EXTERNAL COMPONENTS
  - NO SWR CAPACITOR
  - NO BOOTSTRAP
  - NO BOUCHEROT CELLS
  - INTERNALLY FIXED GAIN
- STAND-BY & MUTE FUNCTIONS
- SHORT CIRCUIT PROTECTION
- THERMAL OVERLOAD PROTECTION

TECHNOLOGY BI20II



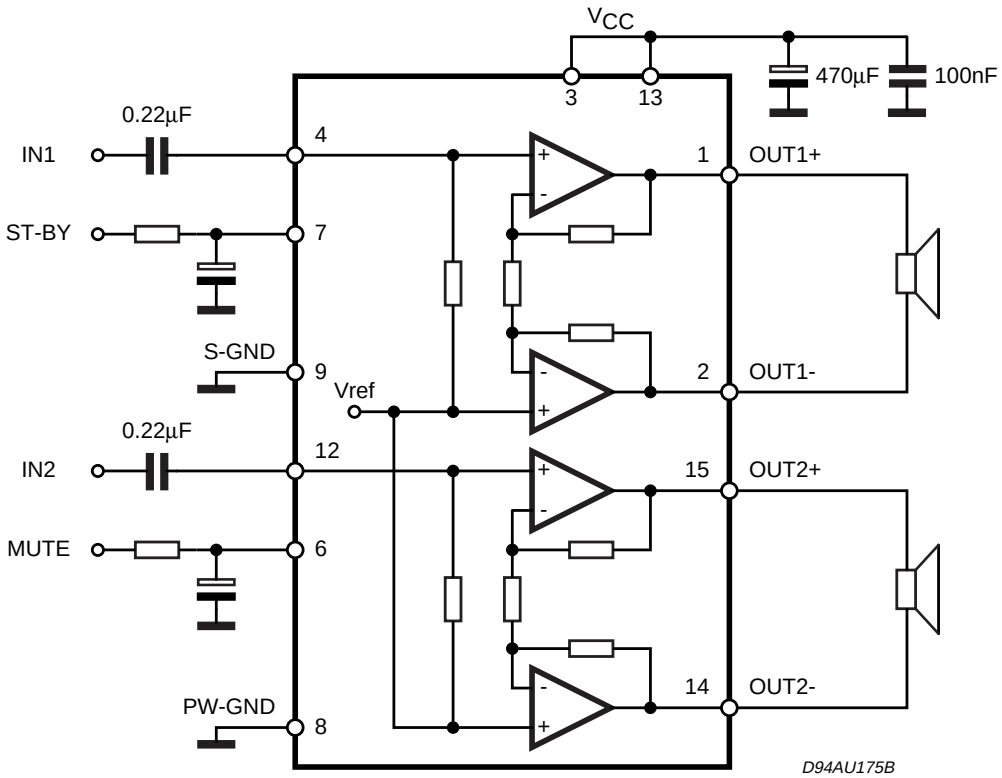
CLIPWATT15
ORDERING NUMBER: TDA7266SA

DESCRIPTION

The TDA7266SA is a dual bridge amplifier specially designed for LCD Monitor, PC Motherboard, TV and Portable Radio applications.

Pin to pin compatible with: TDA7266S, TDA7266, TDA7266M, TDA7266MA, TDA7266B, TDA7297SA & TDA7297.

BLOCK AND APPLICATION DIAGRAM



9.4 TDA7266SA

TDA7266SA

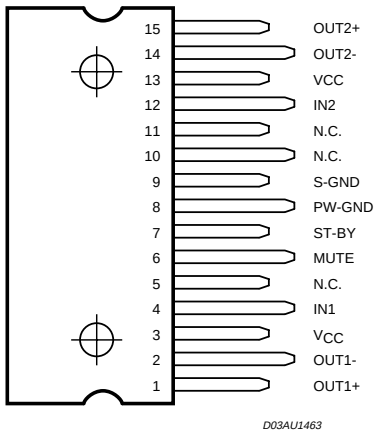
ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_s	Supply Voltage	20	V
I_O	Output Peak Current (internally limited)	2	A
P_{tot}	Total Power Dissipation (T_{amb} = 70°C)	20	W
T_{op}	Operating Temperature	0 to 70	°C
T_{stg}, T_j	Storage and Junction Temperature	-40 to 150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{th\ j\text{-}case}$	Thermal Resistance Junction-case	Typ = 1.8; Max. = 2.5	°C/W
$R_{th\ j\text{-}amb}$	Thermal Resistance Junction-ambient	48	°C/W

PIN CONNECTION (Top view)



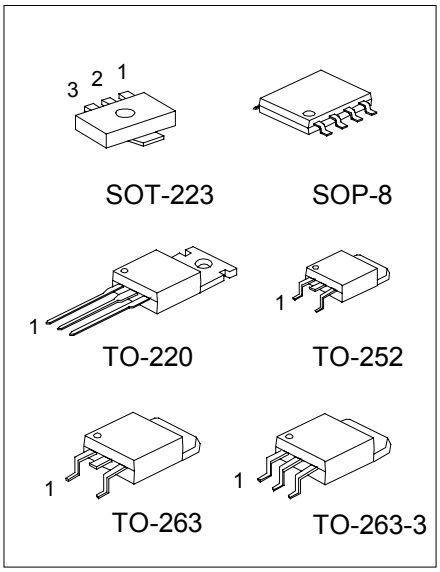
ELECTRICAL CHARACTERISTCS

(V_{CC} = 11V, R_L = 8Ω, f = 1KHz, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply Range		3	11	18	V
I_q	Total Quiescent Current			50	65	mA
V_{OS}	Output Offset Voltage				120	mV
P_O	Output Power	THD 10%	6.3	7		W
THD	Total Harmonic Distortion	P_O = 1W		0.05	0.2	%
		P_O = 0.1W to 2W f = 100Hz to 15KHz			1	%
SVR	Supply Voltage Rejection	f = 100Hz, VR =0.5V	40	56		dB
CT	Crosstalk		46	60		dB
A_{MUTE}	Mute Attenuation		60	80		dB
T_w	Thermal Threshold			150		°C
G_V	Closed Loop Voltage Gain		25	26	27	dB
ΔG_V	Voltage Gain Matching				0.5	dB

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

LOW DROP FIXED AND ADJUSTABLE POSITIVE VOLTAGE REGULATORS



SOP-8 1: GND; 2,3,6,7: Vout;
4: Vin; 5,8: NC

DESCRIPTION

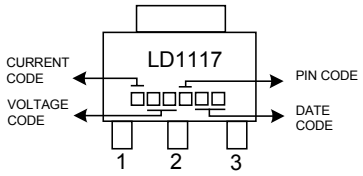
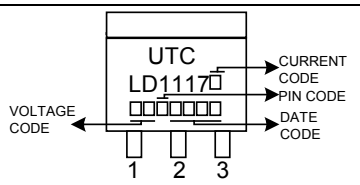
The UTC LD1117/A is a LOW DROP Voltage Regulator able to provide up to 0.8/1.0A of Output Current, available even in adjustable version (Vref=1.25V). Concerning fixed versions, are offered the following Output Voltages: 1.8V, 2.5V, 2.85V, 3.0V, 3.3V and 5.0V. The 2.85V type is ideal for SCSI-2 lines active termination. The device is supplied in: SOT-223, TO-252, TO-263, TO-263-3, SOP-8 and TO-220. The SOT-223, TO-263, TO-263-3 and TO-252 surface mount packages optimize the thermal characteristics even offering a relevant space saving effect. High efficiency is assured by NPN pass transistor. In fact in the case, unlike than PNP one, the Quiescent Current flows mostly into the load. Only a very common 10μF minimum capacitor is needed for stability. On chip trimming allows the regulator to reach a very tight output voltage tolerance, within ±1% at 25°C. The ADJUSTABLE LD1117/A is pin to pin compatible with the other standard Adjustable voltage regulators maintaining the better performances in terms of Drop and Tolerance.

FEATURES

*Low dropout voltage (1V Typ.)
*2.85V device performances are suitable for SCSI-2 active termination
*Output current up to 0.8/1.0A
*Fixed output voltage of: 1.8V,2.5V, 2,85V, 3.0V, 3.3V, 5.0V
*Adjustable version availability (Vref=1.25V)
*Internal current and thermal limit
*Available in ±1%(at 25°C) and 2% in all temperature range
*Supply voltage rejection: 75dB (TYP)
*Temperature range: 0°C to 125°C

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

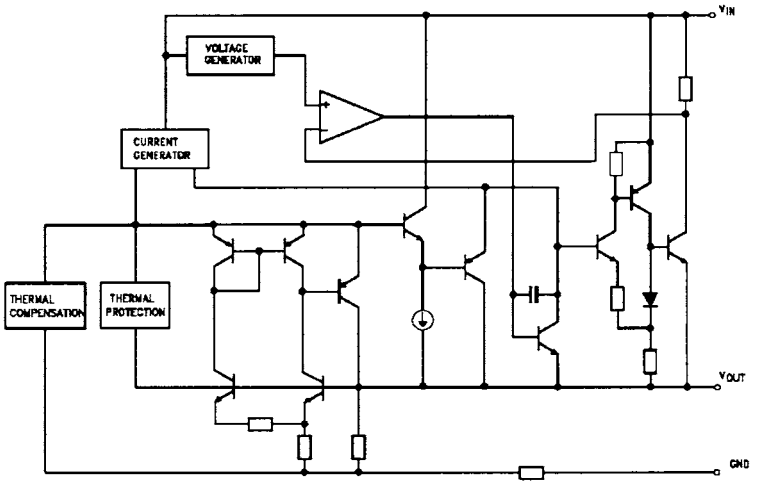
MARKING INFORMATION

PACKAGE	VOLTAGE CODE	PIN CODE	PIN 1	PIN 2	PIN 3	MARKING
SOT-223	18:1.8V 25:2.5V 28:2.85V 30:3.0V 33:3.3V 50:5.0V AD:ADJ	A	GND	OUT	IN	
		B	OUT	GND	IN	
		C	GND	IN	OUT	
		D	IN	GND	OUT	
TO-220 TO-252 TO-263 TO-263-3		A	GND	OUT	IN	
		B	OUT	GND	IN	
		C	GND	IN	OUT	
		D	IN	GND	OUT	

Note: The current code “A” means output current up to 1.0A, while without “A” means output current up to 0.8A.

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
DC Input Voltage	V_{IN}	15	V
Power Dissipation	Ptot	12	W
Storage temperature	Tstg	-65 ~ +150	°C
Operating Junction Temperature	Top	0 ~ +125	°C

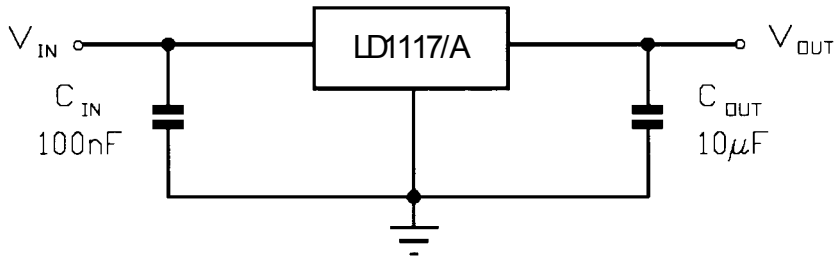
Note: Absolute Maximum Ratings are those value beyond which damage to the device may occur. Functional operation under there condition is not implied. Over the above suggested Max Power Dissipation a Short Circuit could definitively damage the device.

THERMAL DATA

PARAMETER	SYMBOL	VALUE	UNIT
Thermal Resistance Junction-case	Rth-case		
SOT-223		15	°C/W
SOP-8		20	°C/W
TO-252		8	°C/W
TO-220		3	°C/W
TO-263		3	°C/W
Thermal Resistance Junction-ambient	Rthj-amb		
TO-220		50	°C/W

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

APPLICATION CIRCUIT



UTC LD1117/A-1.8 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=3.8V, Io=10mA, Tj=25°C	1.780	1.800	1.820	V
Output Voltage	Vo	Io=0 to 800/1000mA, Vin=3.3 to 8V	1.760		1.840	V
Line Regulation	ΔVo	Vin=3.3 to 8V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=3.3V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			10	V
Quiescent Current	Id	Vin≤8V		5	10	mA
Output Current	Io	Vin=6.8V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.5 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=4.5V, Io=10mA, Tj=25°C	±1%	2.475	2.500	2.525	V
			±2%	2.450	2.500	2.550	V
Output Voltage	Vo	Io=0 to 800/1000mA,	±2%	2.450		2.550	V
		Vin=3.9 to 10V	±4%	2.400		2.600	V
Line Regulation	ΔVo	Vin=3.9 to 10V, Io=0mA			1	6	mV
Load Regulation	ΔVo	Vin=3.9V, Io=0 to 800/1000mA			1	10	mV
Temperature stability	ΔVo				0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C			0.3		%
Operating Input Voltage	Vin	Io=100mA				15	V
Quiescent Current	Id	Vin≤10V			5	10	mA
Output Current	Io	Vin=7.5V, Tj=25°C		800	950	1200	mA

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.5V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-2.85 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=4.85V, Io=10mA, Tj=25°C	2.82	2.85	2.88	V
Output Voltage	Vo	Io=0 to 800/1000mA,Vin=4.25 to 10V	2.79		2.91	V
Line Regulation	ΔVo	Vin=4.25 to 10V, Io=0mA		1	6	mV
Load Regulation	ΔVo	Vin=4.25V, Io=0 to 800/1000mA		1	10	mV
Temperature stability	ΔVo			0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin	Io=100mA			15	V
Quiescent Current	Id	Vin≤10V		5	10	mA
Output Current	Io	Vin=7.85V, Tj=25°C	800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C		100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=5.85V, Vripple=1Vpp	60	75		DB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=5V, Io=10mA, Tj=25°C	±1%	2.97	3.00	3.03	V
			±2%	2.94	3.00	3.06	V
Output Voltage	Vo	Io=0 to 800/1000mA,	±2%	2.94		3.06	V
		Vin=4.5 to 10V	±4%	2.88		3.12	V
Line Regulation	ΔVo	Vin=4.5 to 12V, Io=0mA			1	6	mV
Load Regulation	ΔVo	Vin=4.5V, Io=0 to 800/1000mA			1	10	mV
Temperature stability	ΔVo				0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C			0.3		%
Operating Input Voltage	Vin	Io=100mA				15	V
Quiescent Current	Id	Vin≤12V			5	10	mA
Output Current	Io	Vin=8V, Tj=25°C		800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C			100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6V, Vripple=1Vpp		60	75		dB

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-3.3 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=5.3V, Io=10mA, Tj=25°C	±1%	3.267	3.300	3.333	V
			±2%	3.235	3.300	3.365	V
Output Voltage	Vo	Io=0 to 800/1000mA,	±2%	3.235		3.365	V
		Vin=4.75 to 10V	±4%	3.160		3.440	V
Line Regulation	ΔVo	Vin=4.75 to 15V, Io=0mA			1	6	mV
Load Regulation	ΔVo	Vin=4.75V, Io=0 to 800/1000mA			1	10	mV
Temperature stability	ΔVo				0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C			0.3		%
Operating Input Voltage	Vin	Io=100mA				15	V
Quiescent Current	Id	Vin≤15V			5	10	mA
Output Current	Io	Vin=8.3V, Tj=25°C		800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C			100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=6.3V, Vripple=1Vpp		60	75		DB
Dropout Voltage	Vd	Io=100mA			1.00	1.10	V
		Io=500mA			1.05	1.15	V
		Io=800mA			1.10	1.20	V
		Io=1000mA			1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse			0.01	0.10	%/W

UTC LD1117/A-5.0 ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Output Voltage	Vo	Vin=7V, Io=10mA, Tj=25°C	±1%	4.95	5.00	5.05	V
			±2%	4.90	5.00	5.10	V
Output Voltage	Vo	Io=0 to 800/1000mA,	±2%	4.90		5.10	V
		Vin=6.5 to 15V	±4%	4.80		5.20	V
Line Regulation	ΔVo	Vin=6.5 to 15V, Io=0mA			1	10	mV
Load Regulation	ΔVo	Vin=6.5V, Io=0 to 800/1000mA			1	15	mV
Temperature stability	ΔVo				0.5		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C			0.3		%
Operating Input Voltage	Vin	Io=100mA				15	V
Quiescent Current	Id	Vin≤15V			5	10	mA
Output Current	Io	Vin=10V, Tj=25°C		800	950	1200	mA
Output Noise Voltage	eN	B=10Hz to 10KHz, Tj=25°C			100		μV
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin=8V, Vripple=1Vpp		60	75		dB

UTC LD1117/A LINEAR INTEGRATED CIRCUIT

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

UTC LD1117/A-ADJUSTABLE ELECTRICAL CHARACTERISTICS

(refer to the test circuits, Tj=0 to 125°C, Co=10μF unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Reference Voltage	Vref	Vin-VO=2V, Io=10mA, Tj=25°C	1.238	1.25	1.262	V
Reference Voltage	Vref	Io=10 to 800/1000mA, Vin-Vo=1.4 to 10V	1.225		1.275	V
Line Regulation	ΔVo	Vin-Vo=1.5 to 13.75V, Io=10mA		0.035	0.200	%
Load Regulation	ΔVo	Vin-Vo=3V, Io=10 to 800/1000mA		0.10	0.400	%
Temperature stability	ΔVo			0.50		%
Long Term Stability	ΔVo	1000 hrs, Tj=125°C		0.3		%
Operating Input Voltage	Vin				15	V
Adjustment Pin Current	Iadj	Vin≤15V		60	120	μA
Adjustment Pin Current Change	ΔIadj	Vin-Vo=1.4 to 10V, Io=10 to 800/1000mA		1	5	μA
Minimum Load Current	Io(min)	Vin=15V		2	5	mA
Output Current	Io	Vin-Vo=5V, Tj=25°C	800	950	1200	mA
Output Noise (%Vo)	eN	B=10Hz to 10KHz, Tj=25°C		0.003		%
Supply Voltage Rejection	SVR	Io=40mA, f=120Hz, Tj=25°C, Vin-Vo=3V, Vripple=1Vpp	60	75		dB
Dropout Voltage	Vd	Io=100mA		1.00	1.10	V
		Io=500mA		1.05	1.15	V
		Io=800mA		1.10	1.20	V
		Io=1000mA		1.15	1.25	V
Thermal Regulation		Ta=25°C, 30ms Pulse		0.01	0.10	%/W

TYPICAL APPLICATIONS

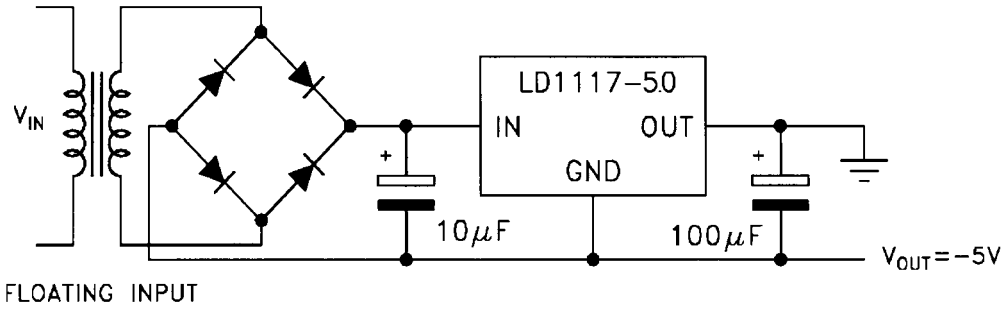


FIG.1 Negative Supply

1.0 General Descriptions

1.1 Introduction

The M260TWR1 is a color active matrix thin film transistor (TFT) liquid crystal display (LCD) that uses amorphous silicon TFT as a switching device. It is composed of a TFT LCD panel, a timing controller, voltage reference, common voltage, DC-DC converter, column driver, and row driver circuit. This TFT LCD has a 26-inch diagonally measured active display area with WXGA resolution (1366 vertical by 768 horizontal pixel array).

1.2 Features

- 26” WXGA TFT LCD Panel
- 4U CCFLs Backlight System
- Supported WXGA (V:1,366 lines, H:768 pixels) resolution
- Compatible with RoHS Standard

1.3 Product Summary

Items	Specifications	Unit
Screen Diagonal	26	inch
Active Area	575.769 (H) x 323.712 (V) `	mm
Pixels H x V	1,366 (x3) x 768	
Pixel Pitch	0.4215 (per one triad) x 0.4215	mm
Pixel Arrangement	R,G,B. Vertical Stripe	
Display Mode	Normally White	
White Luminance	450 typical	cd/m^2 (CCFL@7mA)
Contrast Ratio	1,000 : 1 typical	
Response Time	5 typical	msec
Input Voltage	12 typical	v
Logic Power Consumption	3.6 typical (Black pattern, 60Hz)	watt
Backlight Power Consumption	40 typical (CCFL current 7mA)	watt
Weight	3,900 maximum	g
Outline Dimension	626 (W) x 373 (H) x 32 (T)*	mm
Electrical Interface (Logic)	8 bit LVDS	
Support Color	16.7 M	
Luminance Uniformity(5points)	80% typical	
Optimum Viewing Direction	6 o’clock	
Surface Treatment	Anti Glare + 3H	

*The gibbosities were not calculated in the thickness of the outline dimension.

1.4 Functional Block Diagram

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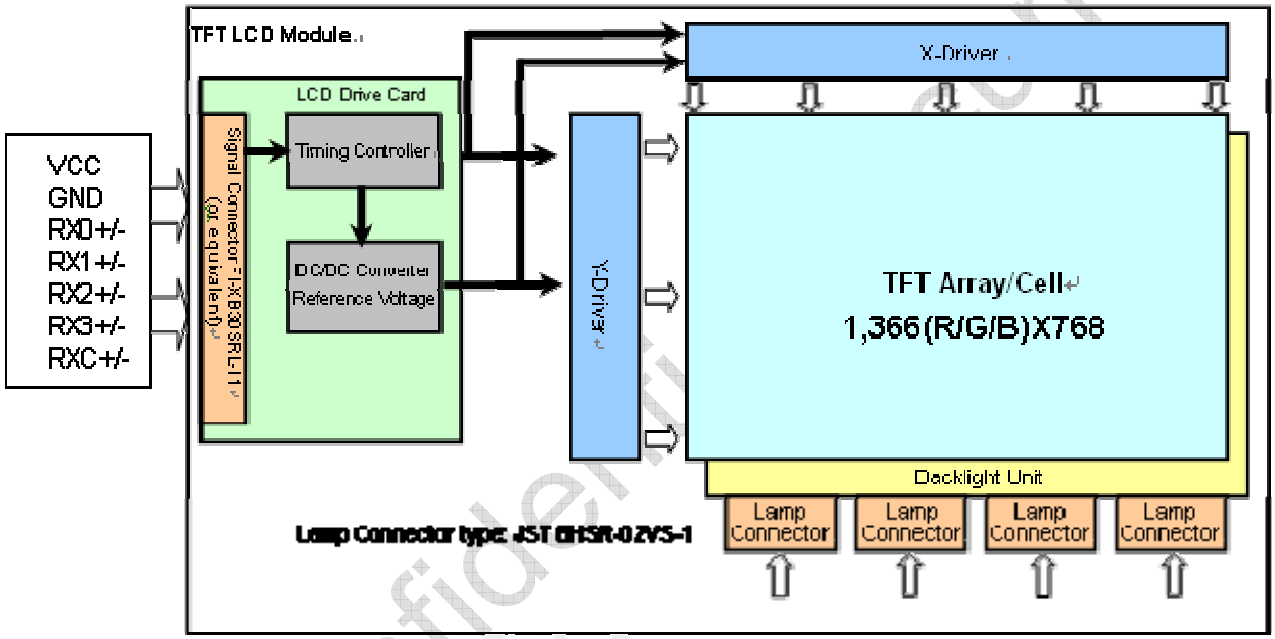
Figure 1 shows the functional block diagram of the LCD module.

Figure 1 Block Diagram



6.0 Electrical Characteristics

6.1 Interface Connector

Table 6 Connector Name / Designation

Manufacturer	UJU (or Equivalent)
Type / Part Number	UJU IS100-L30B-C23
Mating Receptacle/Part Number	JAE FI-X30H(L), JAE FI-X30C*(L), JAE FI-X30M*

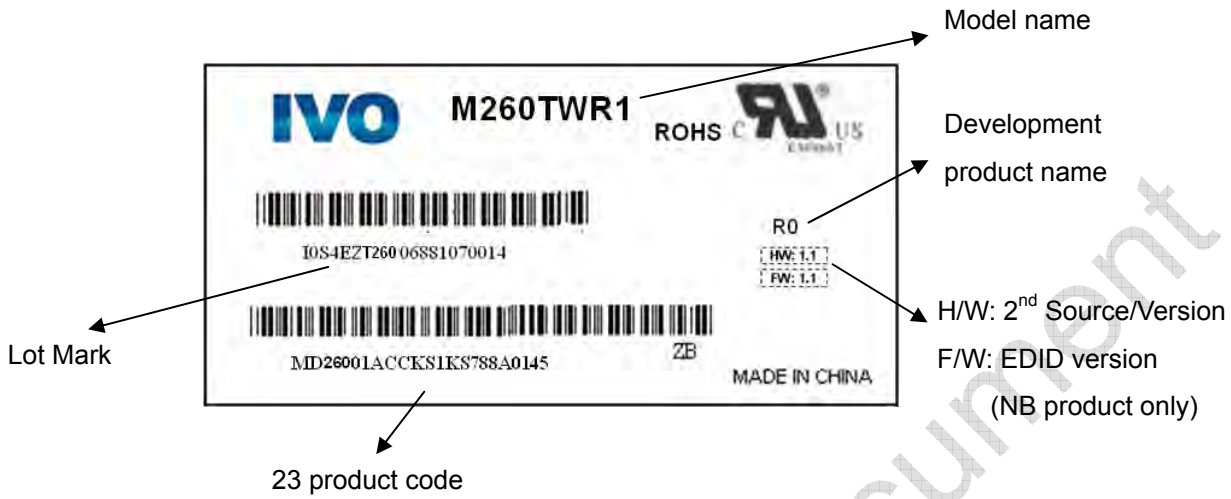
Table 7 Signal Pin Assignment

All input signals shall be low or Hi-Z state when VDD is off.

Pin #	Signal Name	Description	Remarks
1	NC	Not connected	
2	NC	Not connected	
3	NC	Not connected	
4	GND	Ground	
5	RX0-	Negative LVDS differential data input	
6	RX0+	Positive LVDS differential data input	
7	GND	Ground	
8	RX1-	Negative LVDS differential data input	
9	RX1+	Positive LVDS differential data input	
10	GND	Ground	
11	RX2-	Negative LVDS differential data input	
12	RX2+	Positive LVDS differential data input	
13	GND	Ground	
14	RXClk -	Negative LVDS differential clock input	
15	RXClk +	Positive LVDS differential clock input	
16	GND	Ground	
17	RX3-	Negative LVDS differential data input	
18	RX3+	Positive LVDS differential data input	
19	GND	Ground	
20	NC	Not connected	
21	NC	Not connected	
22	TP	Test point	
23	GND	Ground	

24	GND	Ground	
25	GND	Ground	
26	VDD	power supply +12.0V	
27	VDD	power supply +12.0V	
28	VDD	power supply +12.0V	
29	VDD	power supply +12.0V	
30	VDD	power supply +12.0V	

11.0 Lot Mark



11.1 Lot Mark

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20

code 1,2,4,5,6,7,8,9,10,11,16: IVO internal flow control code.
code 3: production location.
code 12: production year.
code 13: production month.
code 14,15: production date.
Code 17,18,19,20: serial number.

Note (1) Production Year

Year	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015
Mark	6	7	8	9	A	B	C	D	F	G

Note (2) Production Month

Month	Jan.	Feb.	Mar.	Apr.	May.	Jun.	Jul.	Aug.	Sep.	Oct	Nov.	Dec.
Mark	1	2	3	4	5	6	7	8	9	A	B	C

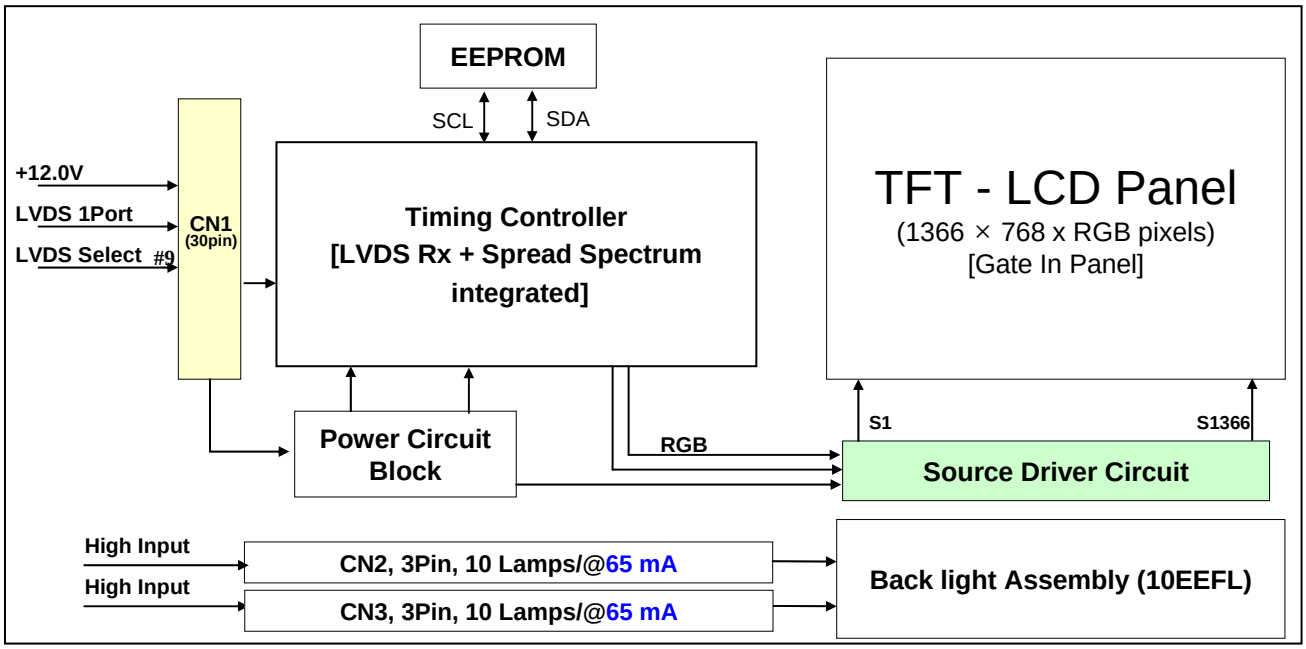
11.2 23 Product Barcode

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23

code 1,2: MD Mindtech Display.
code 3,4,5,6,7: MTDis internal module name.
code 8,9,10,13,16: MTDis internal flow control code.
code 11,12: Cell location Suzhou defined as “SZ”.

1. General Description

The LC320WXE is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive type display operating in the normally black mode. It has a 31.51 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in Horizontal stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot, thus presenting a palette of more than 16.7M(true) colors.
It has been designed to apply the 8-bit 1-port LVDS interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	31.51 inches(800.4mm) diagonal
Outline Dimension	760.0 mm(H) x 450.0 mm(V) x 36.0 mm(D) (Typ.)
Pixel Pitch	510.75㎛ x 170.25㎛ x RGB
Pixel Format	1366 horiz. by 768 vert. pixels RGB horizontal stripe arrangement
Color Depth	8bit, 16,7 M colors
Luminance, White	350 cd/m^2 (Center 1 point) (Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178(Min.), U/D 178(Min.))
Power Consumption	Total 73.5Watt (Typ.) (Logic=3.5 W, Back Light= 70W @ with Inverter)
Weight	4,500g(Typ.) (TBD)
Display Operating Mode	Transmissive mode, normally black
Surface Treatment	Hard coating(3H), anti-glare treatment of the front polarizer **(Haze 10%)**

3-2. Interface Connections

This LCD module employs two kinds of interface connection, a 30-pin connector is used for the module electronics and 2-pin (BDEMR-02VS) (TBD) connector is used for the integral backlight system.

3-2-1. LCD Module

-LCD Connector(CN1) : FI-X30SSL-HF (Manufactured by JAE) or Equivalent
-Mating Connector : FI-X30C2L (Manufactured by JAE) or Equivalent

Table 4. MODULE CONNECTOR(CN5) PIN CONFIGURATION

Pin No.	Symbol	Description	Note
1	V_{LCD}	Power Supply +12.0V	
2	V_{LCD}	Power Supply +12.0V	
3	V_{LCD}	Power Supply +12.0V	
4	V_{LCD}	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	LVDS Select	'H' =JEIDA , 'L' or NC = VESA	**Appendix VII**
10	GND	Ground	
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	PWM OUT	PWM output (From LCM)	
28	Ext V_{BR-B}	External VBR (From System)	
29	GND	Ground	
30	GND	Ground	

Notes : 1. All GND(ground) pins should be connected together to the LCD module's metal frame.
2. All VLCD (power input) pins should be connected together.
3. All Input levels of LVDS signals are based on the EIA 644 Standard. (Please see the Appendix VI)

3-2-2. Backlight Module

[Master]

1) Connector (housing)

: 65002HS-03 (YEONHO) or equivalent

2) Mating Connector (wafer)

: 65002WS-03(YEONHO) or equivalent.

[Slave]

1) Connector (housing)

: 65002HS-03 (YEONHO) or equivalent

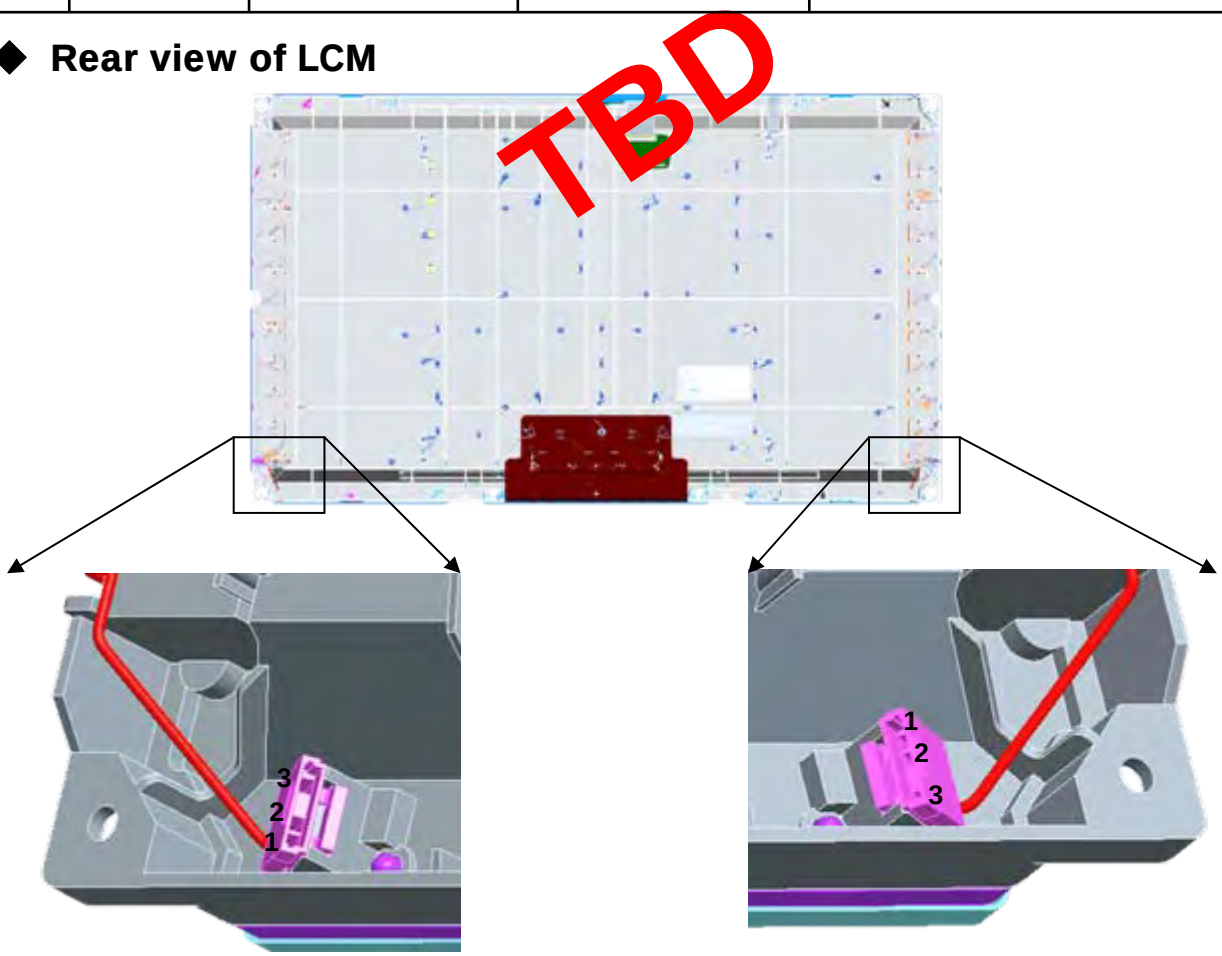
2) Mating Connector (wafer)

: 65002WS-03(YEONHO) or equivalent.

Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN2,CN3)

No	Symbol	Master	Slave	Note
1	**H_Input**	High_Input	High_Input	
2	**H_Input**	High_Input	High_Input	
3	**FB**	NC	NC	

◆ Rear view of LCM



4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and for 60 minutes in a dark environment at 25±2°C. The values are specified at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
FIG. 1 shows additional information concerning the measurement equipment and method.

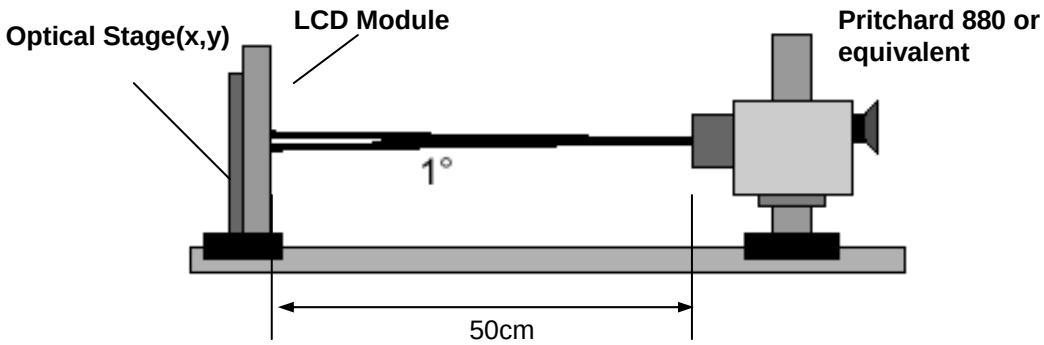


FIG. 1 Optical Characteristic Measurement Equipment and Method

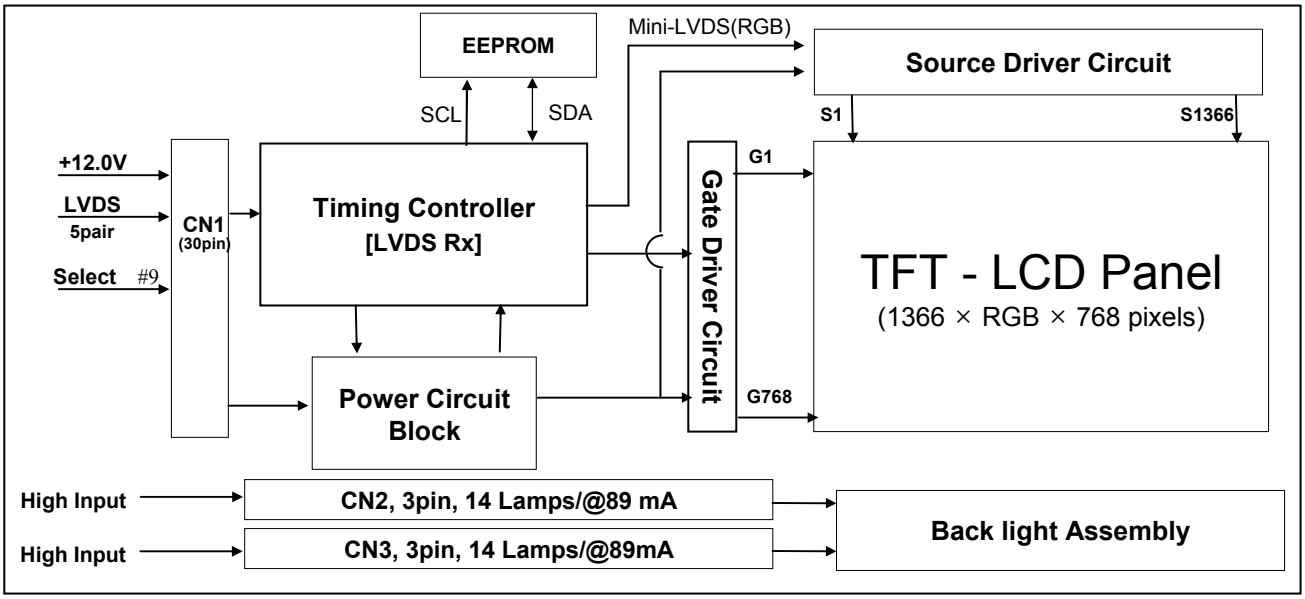
Table 9. OPTICAL CHARACTERISTICS (NOT FIXED)

Ta= 25±2°C, V_{LCD}=12.0V, fv=60Hz, Dclk=72.4MHz, I_{BL}=78mArms

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	700	1000	-		1
Surface Luminance, white		L_{WH}	280	350		cd/m^2	2
Luminance Variation		δ_{WHITE} 5P	-	-	1.3		3
Response Time	ON/OFF		-	22	33	ms	4
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.620	Typ +0.03		
		Ry		0.330			
	GREEN	Gx		0.299			
		Gy		0.592			
	BLUE	Bx		0.148			
		By		0.073			
	WHITE	Wx		0.279			
		Wy		0.292			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	5
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale				2.2			6

1. General Description

The LC370WXE is a Color Active Matrix Liquid Crystal Display with an integral External Electrode Fluorescent Lamp(EEFL) backlight system. The matrix employs a-Si Thin Film Transistor as the active element. It is a transmissive display type which is operating in the normally black mode. It has a 37.02 inch diagonally measured active display area with WXGA resolution (768 vertical by 1366 horizontal pixel array). Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arrayed in vertical stripes. Gray scale or the luminance of the sub-pixel color is determined with a 8-bit gray scale signal for each dot. Therefore, it can present a palette of more than 16.7M(true) colors.
It has been designed to apply the 8-bit 1-port LVDS interface.
It is intended to support LCD TV, PCTV where high brightness, super wide viewing angle, high color gamut, high color depth and fast response time are important.



General Features

Active Screen Size	37.02 inches(940.3mm) diagonal
Outline Dimension	877.0mm(H) x 516.8mm(V) x 46.9mm(D) (Typ.)
Pixel Pitch	0.200mm x 0.600mm x RGB
Pixel Format	1366 horiz. by 768 vert. pixels RGB stripe arrangement
Color Depth	8-bit, 16.7 M colors
Luminance, White	380 cd/m^2 (Center 1 point Typ.)
Viewing Angle (CR>10)	Viewing angle free (R/L 178(Typ.), U/D 178(Typ.))
Power Consumption	Total 88.2 Watt (Typ.) (Logic= 3.2 W, Inverter= 85W @ with inverter)
Weight	6,950(Typ.)
Display Mode	Transmissive mode, Normally black
Surface Treatment	Hard coating(3H), Anti-glare treatment of the front polarizer (Haze 13%)

3-2. Interface Connections

This LCD module employs two kinds of interface connection, a 30-pin connector is used for the module electronics and 3-pin Balance PCB connector is used for the integral backlight system.

3-2-1. LCD Module

- LCD Connector(CN5) : FI-X30SSL-HF (Manufactured by JAE) or IS100-L30B-C23(Manufactured by UJU)
- Mating Connector : FI-X30C2L (Manufactured by JAE) or Equivalent

Table 4. MODULE CONNECTOR(CN5) PIN CONFIGURATION

Pin No.	Symbol	Description	Note
1	VLCD	Power Supply +12.0V	
2	VLCD	Power Supply +12.0V	
3	VLCD	Power Supply +12.0V	
4	VLCD	Power Supply +12.0V	
5	GND	Ground	
6	GND	Ground	
7	GND	Ground	
8	GND	Ground	
9	LVDS Select	'H' =JEIDA , 'L' or NC = VESA	**Appendix VII**
10	NC	No Connection	
11	GND	Ground	
12	RA-	LVDS Receiver Signal(-)	
13	RA+	LVDS Receiver Signal(+)	
14	GND	Ground	
15	RB-	LVDS Receiver Signal(-)	
16	RB+	LVDS Receiver Signal(+)	
17	GND	Ground	
18	RC-	LVDS Receiver Signal(-)	
19	RC+	LVDS Receiver Signal(+)	
20	GND	Ground	
21	RCLK-	LVDS Receiver Clock Signal(-)	
22	RCLK+	LVDS Receiver Clock Signal(+)	
23	GND	Ground	
24	RD-	LVDS Receiver Signal(-)	
25	RD+	LVDS Receiver Signal(+)	
26	GND	Ground	
27	NC	No Connection	
28	NC	No Connection	
29	GND	Ground	
30	GND	Ground	

Notes :
1. All GND(ground) pins should be connected together to the LCD module's metal frame.
2. All VLCD (power input) pins should be connected together.
3. All Input levels of LVDS signals are based on the **EIA 644** Standard. (Please see the Appendix VI)
4. Specific pin No. **#30** is used for "No signal detection" of system signal interface.
   It should be GND for **NSB(No Signal Black)** during the system interface signal is not.
   If this pin is "H", LCD Module displays **AGP(Auto Generation Pattern).**

3-2-2. Backlight Inverter

[Master]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO)or equivalent

2) Mating Connector

: 65002HS-03 (manufactured by YEONHO) or equivalent.

[Slave]

1) Balance Connector

: 65002WS-03 (manufactured by YEONHO)or equivalent

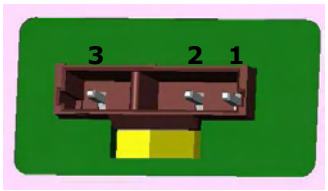
2) Mating Connector

: 65002HS-03 (manufactured by YEONHO) or equivalent.

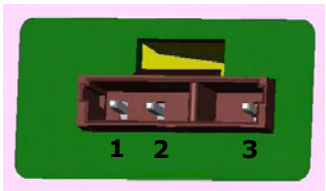
Table 5. BACKLIGHT CONNECTOR PIN CONFIGURATION(CN2,CN3)

No	Symbol	Master	Slave	Note
1	**H_Input**	High_Input	High_Input	
2	**H_Input**	High_Input	High_Input	
3	**FB**	NC	NC	

◆ Rear view of LCM



Master



Slave

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable in a dark environment at 25±2°C. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of Φ and θ equal to 0 °.
FIG. 1 shows additional information concerning the measurement equipment and method.

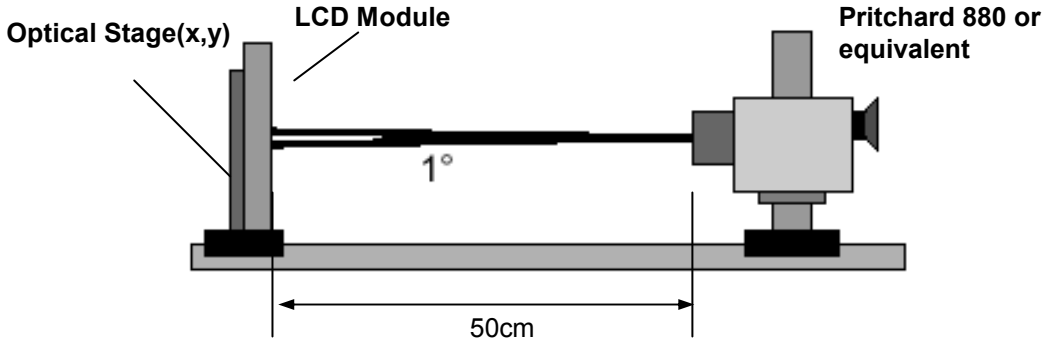


FIG. 1 Optical Characteristic Measurement Equipment and Method

Table 10. OPTICAL CHARACTERISTICS Ta= 25±2°C, V_{LCD}=12.0V, fv=60Hz, Dclk=72.4MHz, I_{BL}=89mArms

Parameter		Symbol	Value			Unit	Note
			Min	Typ	Max		
Contrast Ratio		CR	800	1200	-		1
Surface Luminance, white		L_{WH}	304	380	-	cd/m²	2
Luminance Variation		δ_{WHITE} 5P	-	-	1.3		3
Response Time	Gray-to-Gray	G to G	-	8	12	ms	4
	Uniformity	G to G σ	-	6	9		5
Color Coordinates [CIE1931]	RED	Rx	Typ -0.03	0.636	Typ +0.03		
		Ry		0.335			
	GREEN	Gx		0.290			
		Gy		0.610			
	BLUE	Bx		0.144			
		By		0.063			
	WHITE	Wx		0.279			
		Wy		0.292			
Viewing Angle (CR>10)							
	x axis, right(ϕ=0°)	θr	89	-	-	degree	6
	x axis, left (ϕ=180°)	θl	89	-	-		
	y axis, up (ϕ=90°)	θu	89	-	-		
	y axis, down (ϕ=270°)	θd	89	-	-		
Gray Scale			-	2.2	-		7

1. General Description

This specification applies to the 42.0 inch Color TFT-LCD Module T420HW06 V3. This LCD module has a TFT active matrix type liquid crystal panel 1,920x1,080 pixels, and diagonal size of 42.0 inch. This module supports 1,920x1,080 mode. Each pixel is divided into Red, Green and Blue sub-pixels or dots which are arranged in vertical stripes. Gray scale or the brightness of the sub-pixel color is determined with a 8-bit gray scale signal for each dot.

The T420HW06 V3 has been designed to apply the 8-bit 2 channel LVDS interface method. It is intended to support displays where high brightness, wide viewing angle, high color saturation, and high color depth are very important.

*** General Information**

Items	Specification	Unit	Note
Active Screen Size	42.02	inch	
Display Area	930.24(H) x 523.26(V)	mm	
Outline Dimension	983.0(H) x 576.0(V) x 49(D)	mm	
Driver Element	a-Si TFT active matrix		
Display Colors	16.7M	Colors	
Number of Pixels	1920X1080	Pixel	
Pixel Pitch	0.4845	mm	
Pixel Arrangement	RGB vertical stripe		
Display Operation Mode	Normally Black		
Surface Treatment	Anti-Glare, 3H		Haze=13%

3.2 Interface Connections

- LCD connector: 187059-51221 (P-TWO, LVDS connector)
- Mating connector:

PIN	Symbol	Description	PIN	Symbol	Description
1	GND	Ground	26	GND	Ground
2	NC	No connection	27	GND	Ground
3	Reserved	AUO Internal Use Only	28	CH2_0-	LVDS Channel 2, Signal 0-
4	Reserved	AUO Internal Use Only	29	CH2_0+	LVDS Channel 2, Signal 0+
5	NC	No connection	30	CH2_1-	LVDS Channel 2, Signal 1-
6	Reserved	AUO Internal Use Only	31	CH2_1+	LVDS Channel 2, Signal 1+
7	LVDS_SEL	Open/High(3.3V) for NS, Low(GND) for JEIDA	32	CH2_2-	LVDS Channel 2, Signal 2-
8	Reserved (VBR_EXT)	PWM Dimming signal input (AC : 0~3.3V, max:4V, Duty : 60~100%, freq : 120~240Hz)	33	CH2_2+	LVDS Channel 2, Signal 2+
9	Reserved (OPC_OUT)	PWM Dimming signal output (AC:0~3.3V)	34	GND	Ground
10	Reserved (OPC Enable)	Enable DCR function Enable:3.3V(max:4V), Disable:0V(or Open)	35	CH2_CLK-	LVDS Channel 2, Clock -
11	GND	Ground	36	CH2_CLK+	LVDS Channel 2, Clock +
12	CH1_0-	LVDS Channel 1, Signal 0-	37	GND	Ground
13	CH1_0+	LVDS Channel 1, Signal 0+	38	CH2_3-	LVDS Channel 2, Signal 3-
14	CH1_1-	LVDS Channel 1, Signal 1-	39	CH2_3+	LVDS Channel 2, Signal 3+
15	CH1_1+	LVDS Channel 1, Signal 1+	40	Reserved	AUO Internal Use Only
16	CH1_2-	LVDS Channel 1, Signal 2-	41	Reserved	AUO Internal Use Only
17	CH1_2+	LVDS Channel 1, Signal 2+	42	GND	Ground
18	GND	Ground	43	GND	Ground
19	CH1_CLK-	LVDS Channel 1, Clock -	44	GND	Ground
20	CH1_CLK+	LVDS Channel 1, Clock +	45	GND	Ground
21	GND	Ground	46	GND	Ground
22	CH1_3-	LVDS Channel 1, Signal 3-	47	NC	No connection
23	CH1_3+	LVDS Channel 1, Signal 3+	48	V_{DD}	Power Supply, +12V DC Regulated
24	Reserved	AUO Internal Use Only	49	V_{DD}	Power Supply, +12V DC Regulated
25	Reserved	AUO Internal Use Only	50	V_{DD}	Power Supply, +12V DC Regulated
			51	V_{DD}	Power Supply, +12V DC Regulated

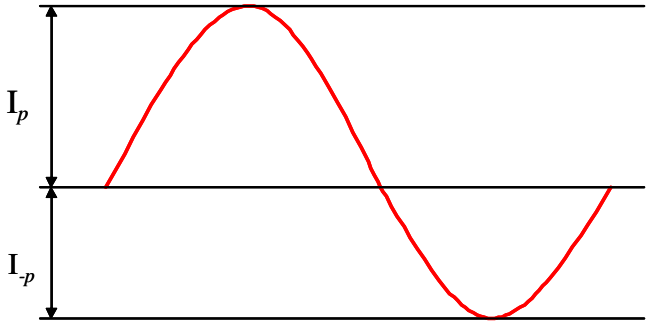
3.7.2 lamp specification

Item	Symbol	Condition	Spec			Unit	Note
			Min	Typ	Max		
Lamp voltage	VL		800	1000	1200	Vrms	1
Lamp current	IL		-	13	-	mArms	
Lamp frequency	fL		35		80	kHz	
Starting voltage	Vs	At 0℃	-	-	1840	Vrms	
		At 25℃	-	-	1157	Vrms	
Delayed discharge time	TD		-	-	0.5	sec	
Life time	TL		50K	-	-	hr	
Unsymmetrical ratio	UR		-	-	10%	-	Note 1.
Crest factor	C.F.		$\sqrt{2}-10\%$	$\sqrt{2}$	$\sqrt{2}+10\%$	-	

The above characteristics are measured under the conditions:
Ambient temperature: 25±2℃, Relative Humidity: 65±20%RH.

Note 1: Waveform definition

Please light on the lamp with symmetrical voltage and current waveform (unsymmetrical ratio is less than 10%, crest factor within $\sqrt{2}\pm10\%$).



Unsymmetrical Ratio = $|I_p - I_{-p}| / I_{rms} * 100\%$

Crest Factor = I_p (or I_{-p}) / I_{rms}

I_p : High side peak value

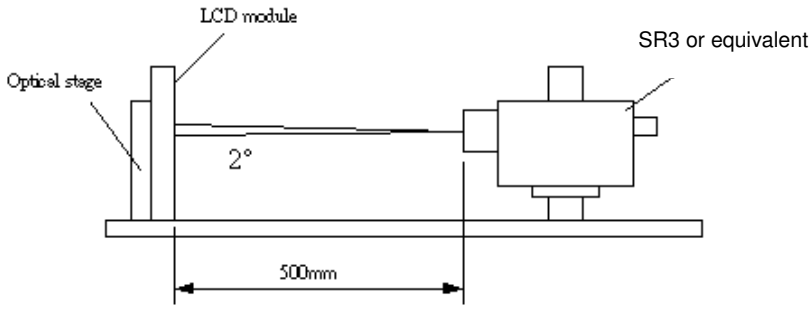
I_{-p} : Low side peak value

I_{rms} : Root mean square value

4. Optical Specification

Optical characteristics are determined after the unit has been 'ON' and stable for approximately 45 minutes in a dark environment at 25℃. The values specified are at an approximate distance 50cm from the LCD surface at a viewing angle of φ and θ equal to 0°.

Fig.1 presents additional information concerning the measurement equipment and method.



Parameter		Symbol	Values			Unit	Notes
			Min.	Typ.	Max		
Contrast Ratio		CR	3200	4000	--		1
Surface Luminance (White)		L_{WH}	380	450	--	cd/m^2	2
Luminance Variation		$\delta_{WHITE(9P)}$	--	--	1.3		3
Response Time (G to G)		Tγ	--	8	--	Ms	4
Color Gamut		NTSC		72		%	
Color Coordinates							
	Red	R_X	Typ.-0.03	0.640	Typ.+0.03		
		R_Y		0.330			
	Green	G_X		0.281			
		G_Y		0.590			
	Blue	B_X		0.144			
		B_Y		0.060			
	White	W_X		0.280			
		W_Y		0.290			
Viewing Angle							5
	x axis, right(φ=0°)	θ_r	--	89	--	degree	
	x axis, left(φ=180°)	θ_l	--	89	--	degree	
	y axis, up(φ=90°)	θ_u	--	89	--	degree	
	y axis, down (φ=270°)	θ_d	--	89	--	degree	

Note:

8. Pin Connection（连接器脚位定义）

Table 15 Pin-CN3 Connection And Function

NO.	Pin Connection	Function
1	+5VSB	STANDBY OUTPUT
2.3	+12V	+12V OUTPUT
4.5	GND	GND RETURN
6.7	5V	+5V OUTPUT
8.9	GND	GND RETURN
10	SB	SMPS ON/OFF CONTROL(ON = HIGH)
11	BK	BACKLIGHT ON
12	DM	INTERNAL PWM DIMMING

Note: CN3 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 16 Pin-CN10 Connection And Function

NO.	Pin Connection	Function
1	GND	+5V RETURN
2	GND	+5V RETURN
3.4.7.8	+5V	+5V OUTPUT
5	SB	SMPS ON/OFF CONTROL(ON = HIGH)
6	+VS	STANDBY OUTPUT
9.10.11	GND	+VS. +12V RETURN
12.13	+12V	+12V OUTPUT

Note: CN10 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 17 Pin-CN11 Connection And Function

NO.	Pin Connection	Function
1	GD	GND
2	SB	SMPS ON/OFF CONTROL(ON = HIGH)
3	DM	INTERNAL PWM DIMMING
4	BK	BACKLIGHT ON
5	PM	EXTERNAL PWM DIMMING DUTY

Note: CN11 -- JST VA CONNEETION, TYPE : pitch2.0mm

Table 18 Pin-CN4；CN5；CN6；CN7 Connection And Function

NO.	Pin Connection	Function
1、2	CCFL	CCFL-VOL. Output

Note:

Table 19 Pin-CN2 Connection And Function

NO.	Pin Connection	Function
1	AC-N2009	AC INPUT NUTURE FROM SW
2	NC	NC
3	AC-L2	AC INPUT LINE FROM SW
4	NC	NC
5	AC- N1	AC INPUT LINE TO SW
6	NC	NC
7	AC- L1	AC INPUT NUTURE TO SW

Note: CN2 -- JST VA CONNEETION, TYPE : pitch3.96mm

Table 20 Pin-CN1 Connection And Function

NO.	Pin Connection	Function
①	AC-N	AC INPUT NUTURE
②	NC	NC
③	AC-L	AC INPUT LINE

Note: CN1 -- JST VA CONNEETION, TYPE : pitch3.96mm

Table 21 Pin-CN8 Connection And Function

Pin Connection	Function
PIN① AND PIN② SHORT	EXTERNAL PWM DIMMING DUTY ENABLE
PIN①AND PIN② OPEN	INTERNAL PWM DIMMING

Note: CN8 -- JST VA CONNEETION, TYPE : pitch2.54mm

5.6 Shock（冲击耐受）

* 49m/s²(5G),11ms, once each X, Y and Z axis.

6. Dimension （物理尺寸）

*230 mm X 120mm X 25mm(元件面高) (长 L *宽 W * 高 H).

7. Weight （重量）

8. Pin Connection (连接器脚位定义)

Table 13 CN2(10Pin)

NO.	Pin Connection	Function
1	+12V	+12V DC OUTPUT
2	+12V	+12V DC OUTPUT
3	SGND	RETURN
4	SGND	RETURN
5	+5V	+5V OUTPUT
6	+5V	+5V OUTPUT
7	SGND	RETURN
8	SGND	RETURN
9	+5VSB	+5V OUTPUT
10	STB	SMPS ON/OFF CONTROL(ON = HIGH)

Note: DOUBLE ROW CONNEETION, pitch:2.5mm.

Table 14 CN3(4Pin)

NO.	Pin Connection	Function
1	+24V	+24V DC OUTPUT
2	+24V	+24V DC OUTPUT
3	SGND	RETURN
4	SGND	RETURN

Note: DOUBLE ROW CONNEETION, pitch:2.5mm

Table 15 CN7(4Pin)

NO.	Pin Connection	Function
1	BK	BACKLIGHT ON
2	DM	INTERNAL PWM DIMMING
3	NC	NC

4	SGND	RETURN

Note: DOUBLE ROW CONNEETION, pitch:2.0mm

Table 16 CN1(3Pin)

NO.	Pin Connection	Function
1	AC-L	AC INPUT LINE
2	NC	NC
3	AC-N	AC INPUT NUTURE

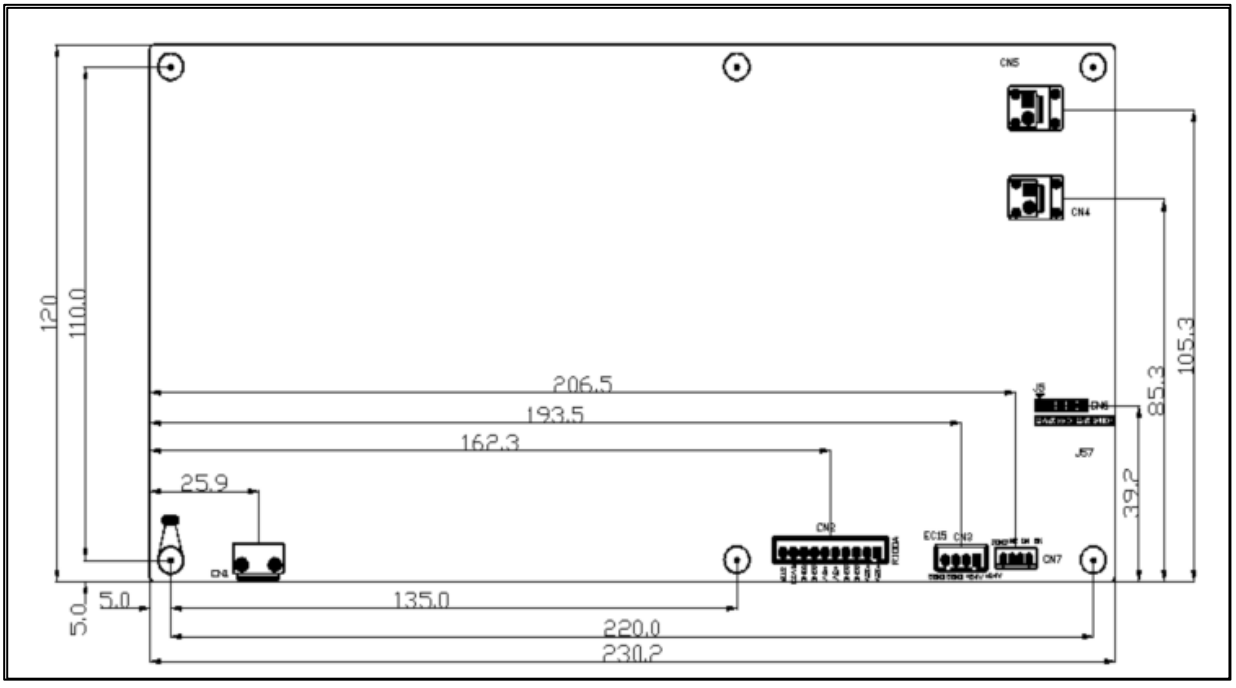
Note: DOUBLE ROW CONNEETION, pitch:3.96mm

Table 17 CN4,CN5(2Pin)

NO.	Pin Connection	Function
1,2	EEFL	EEFL-VOL. Output

Note: DOUBLE ROW CONNEETION, pitch:3.96mm

9. Power Supply Mounting （安装尺寸）单位 mm.



* 10-55Hz, 19.6m/s² (2G), 3minutes period, 60minutes each along X, Y and Z axis.

5.6 Impact （冲击耐受）

* 49m/s² (5G),11ms, once each X, Y and Z axis.

6. Dimension （物理尺寸）

* 205mm X 133mm X 30mm (长 L *宽 W * 元件高 H).

7. Weight （重量）

8. Pin Connection（连接器脚位定义）

Table 15 Pin-CN3 Connection And Function

NO.	Pin Connection	Function
1	EPWM-IN	EXTERNAL PWM DIMMING DUTY
2	BK	BACKLIGHT ON/OFF
3	APWM	INTERNAL PWM DIMMING
4	STB	SMPS ON/OFF CONTROL(ON = HIGH)
5	GND	GND RETURN

Note: CN3 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 16 Pin-CN4 Connection And Function

NO.	Pin Connection	Function
1	+5VSB	STANDBY OUTPUT
2.3.4.5	+12V	+12V OUTPUT
6.7.8.9	GND	GND RETURN
10	STB	SMPS ON/OFF CONTROL(ON = HIGH)
11	BK	BACKLIGHT ON/OFF
12	APWM	INTERNAL PWM DIMMING

Note: CN4 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 17 Pin-CN5 Connection And Function

NO.	Pin Connection	Function
1.2	GND	GND RETURN
3.4	+5V	+5V OUTPUT
5	STB	SMPS ON/OFF CONTROL(ON = HIGH)
6	+5VSB	STANDBY OUTPUT
7.8	+5V	+5V OUTPUT
9.10.11	GND	GND RETURN
12.13	+12V	+12V OUTPUT

Note: CN5 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 18 HV Function

NO.	Pin Connection	Function
HV	TFT	TFT-VOL. Output

Note:

Table 19 Pin-CN1 Connection And Function

NO.	Pin Connection	Function
①	AC-N	AC INPUT NUTURE
②	NC	NC
③	AC-L	AC INPUT LINE

Note: CN1 -- JST VA CONNEETION, TYPE : pitch3.96mm

Table 20 Pin-CN2 Connection And Function

Pin Connection	Function
PIN① AND PIN② SHORT	EXTERNAL PWM DIMMING DUTY ENABLE
PIN①AND PIN② OPEN	INTERNAL PWM DIMMING

Note: CN2 -- JST VA CONNEETION, TYPE : pitch2.54mm

Table 21 Pin-CN7 Connection And Function

NO.	Pin Connection	Function
1	HVGND1	HVGND1
2.3	NC	NC
4	VS1	VS1
5	GND	GND
6.7.8	A2	A2
9.10.11	A1	A1

Note: CN7 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 22 Pin-CN8 Connection And Function

NO.	Pin Connection	Function
1	HVGND2	HVGND2
2.3	NC	NC
4	VS2	VS2
5	GND	GND
6.7.8	A1	A1
9.10.11	A2	A2

Note: CN8 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 23 Pin-CN1A Connection And Function

NO.	Pin Connection	Function
1	HVGND	HVGND
2.3	NC	NC
4	VS	VS
5	GND	GND
6.7.8	A1	A1
9.10.11	A2	A2

Note: CN1A -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 16 Pin-CN4 Connection And Function

NO.	Pin Connection	Function
1	STB	SMPS ON/OFF CONTROL(ON = HIGH)
2.4.6.8.9	GND	GND RETURN
3	+5VSB	STANDBY OUTPUT
5.7	+12V	+12V OUTPUT
10.11	+24V	+24V OUTPUT

Note: CN4 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 17 Pin-CN9 Connection And Function

NO.	Pin Connection	Function
1	STB	SMPS ON/OFF CONTROL(ON = HIGH)
2	+5VSB	STANDBY OUTPUT
3,4 ,7,9,10	GND	GND RETURN
5,6	+5V	+5V OUTPUT
8	+12V	+12V OUTPUT
11, 12	+24V	+24V OUTPUT

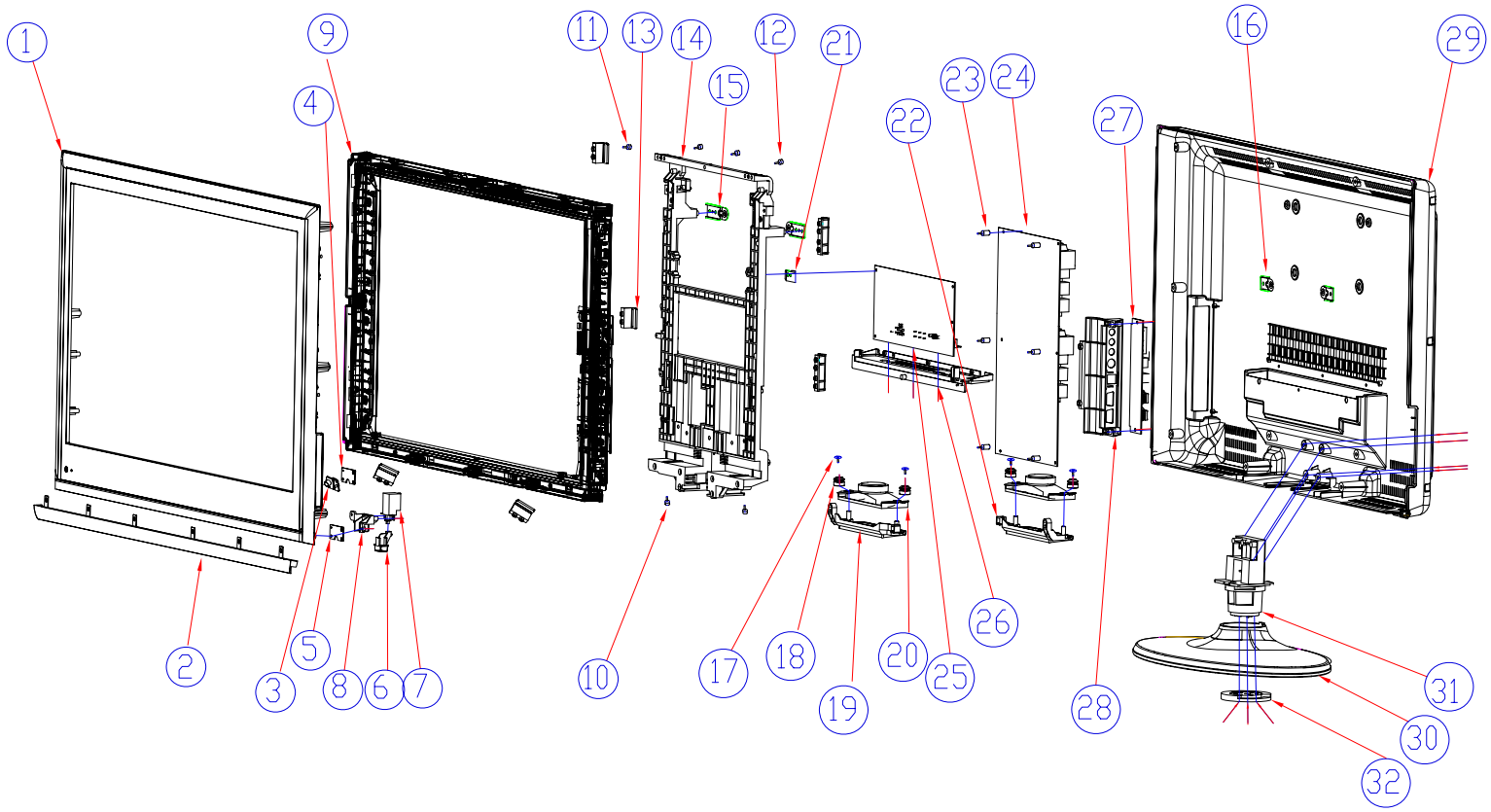
Note: CN5 -- JST VA CONNEETION, TYPE : pitch2.5mm

Table 18 Pin-CN1 Connection And Function

NO.	Pin Connection	Function
1	AC-N	AC INPUT NUTURE
2,3,4	NC	NC
5	AC-L	AC INPUT LINE

Note: CN1 -- JST VA CONNEETION, TYPE : pitch3.96mm,

版本	区域	内容/概述	日期	签名
1		3201爆炸图		卢权均



序号	物料编号	名称	数量
32	54-L32010-270	L3201法兰盘	1
31	54-L32010-260	L3201转轴	1
30	54-L32010-110	L3201底座	1
29	52-0L3201-300	L3201后盖	1
28	54-L32010-242	L3201侧AV支架-M3	1
27	82-L320S6-AVY	L3201-S6 STDE AVIN组件	1
26	54-L3201S-024	L3201(SD)端子板	1
25	82-L321SD-MAY01AI	SD机芯板成品	1
24	R41-PDWMIP-260	26"电源+升压板MIP260B-19 ROHS	1
23	57-W30060-108	铜柱	1
22	54-L3201R-240	L3201(R)喇叭支架(右)	1
21	59-L3201R-0G06	机芯支撑铁条L3201R-0G06(优化后通用)	1
20	82-3201L4-LB01	L3201-L4机芯喇叭组件	1
19	54-L3201L-240	L3201(L)喇叭支架(左)	1
18	55-100550-000	21A8喇叭胶垫(Φ14 *Φ6.5 * h11)mm	4
17	56-V30120-AB3	自攻螺钉PWA3*12(Φ12黑)	4
16	59-L2601U-0G02	L2601壁挂支架	2
15	59-L3201Q-0G01	L3201壁挂支架	2
14	54-0L2601-010	L2601主支架	1
13	59-L2601W-0G02	压屏件L2601-B(H=18.5mm)	2
12	56-T40160-BT6	自攻螺钉TT4×16(黑 加硬)	27
11	56-T40120-AB7	自攻螺钉TA4×12(彩 加硬)	6
10	57-B40100-103	机制螺钉DM4*10(黑)	4
9	R32-LCD26T-IV01	26"液晶屏M260TWR1 R1_V00 ROHS(客户提供)	1
8	54-L26010-242	L2601开关支架	1
7	82-L3201E-PKY01	L3201-S9 VDE电源开关组件(II类)	1
6	54-L26010-070	L2601电源钮(啞黑色)	1
5	82-3201S9-FBY	L3201-S9控制板组件(带屏蔽)	1
4	82-3201S9-IRY	L3201-S9接收板组件(单红灯)	1
3	54-L32010-160	L3201导光柱	1
2	54-0L2601-170	L2601装饰条	1
1	52-0L2601-100	L2601前座	1

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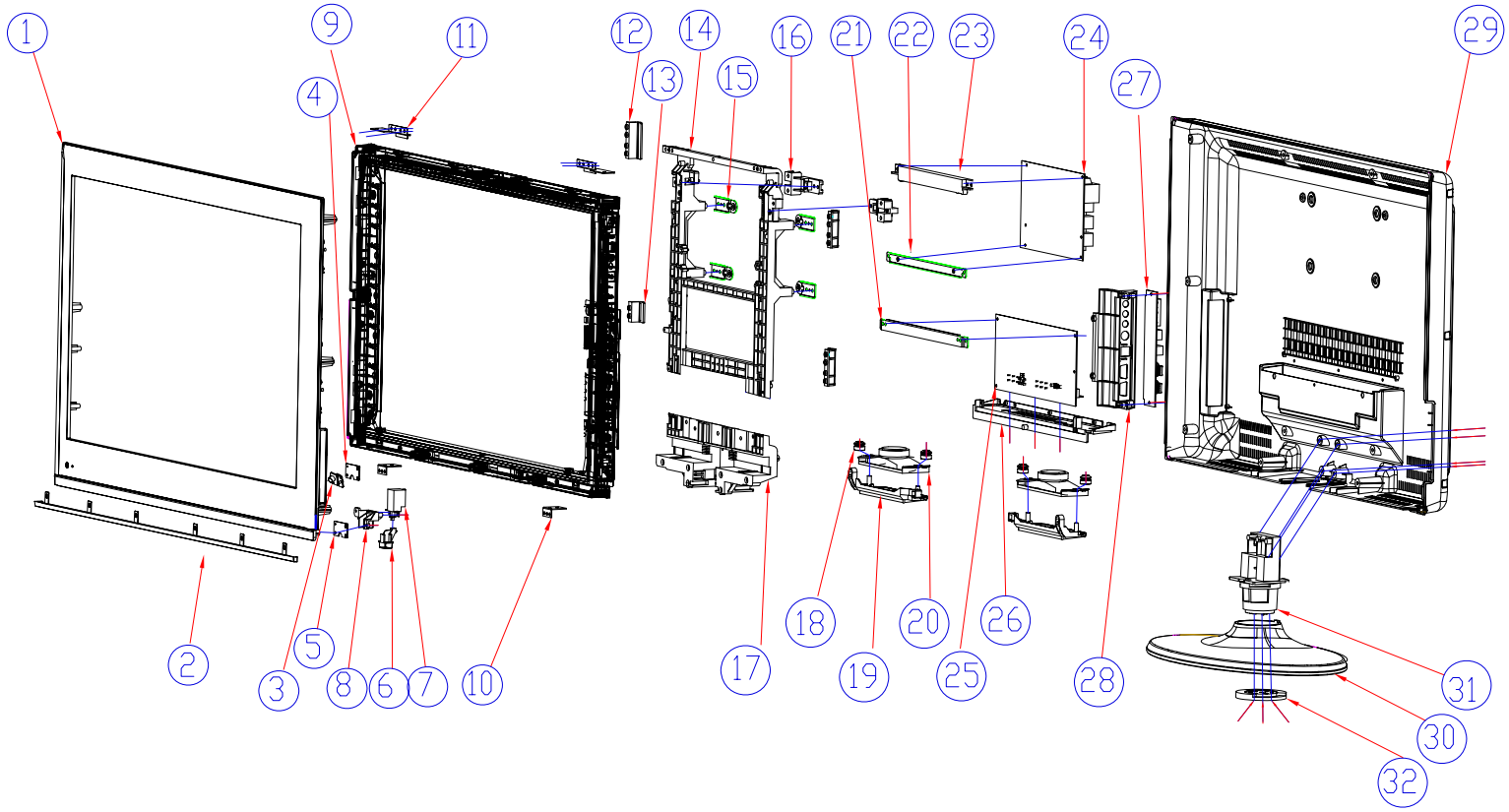
设 计			零件名称:	2601爆炸图	产品型号:		
审 核			物料编号:				
标准化			材 料:		单位	mm	比 例	
核准			表面处理:		数量		质 量	
公 差	0 ~ 30	±0.10	>30~100	±0.20	第 张 共 张			
	>100	±0.30	ANGULAR:	± 0.3°				
A2	3rd ANGLE PROJECTION				JPE 珠海经济特区金品电器有限公司			

版本	区域	内容/概述	日期	签名
1		3201爆炸图		卢权均



序号	物料编号	名称	数量
32	54-L32010-270	L3201法兰盘	1
31	54-L32010-260	L3201转轴	1
30	54-L32010-110	L3201底座	1
29	52-0L3201-300	L3201后盖	1
28	54-L32010-242	L3201侧AV支架-M3	1
27	82-L320S9-AVY	L3201-S9 Side AVIN+USB组件	1
26	54-L3201S-020	L3201(S9)端子板	1
25	82-L42PS9-MAY01	L42PIS9-KW MST6E16(PAL)机芯成品(12V供	1
24	R41-PDWHDZ-180	电源HDZ1804-3A ROHS	1
23	54-L32010-240	L3201电源板支架(阻燃料)	1
22	59-L3201R-0G01	L3201电源板支撑铁条	1
21	59-L3201R-0G02	L3201机芯板支撑铁条	1
20	82-3201L4-LB01	L3201-L4机芯喇叭组件	1
19	54-L3201L-240	L3201(L)喇叭支架(左)	1
18	55-100550-000	21A8喇叭胶垫(Φ14 *Φ6.5 * h11)mm	4
17	54-L32010-252	L3201支撑架	2
16	54-L32010-250	L3201(L)连屏件	2
15	59-L3201Q-0G01	L3201壁挂支架	4
14	54-L32010-010	L3201主支架	1
13	54-L3201S-251	L3201(S)压屏件(H=17.5mm)	2
12	54-L3201L-251	L3201(L)压屏件(H=17.5mm)	3
11	59-L3201W-0G03	压屏件3201-0G03	1
10	59-L3201P-0G02	L3201侧锁件(H=17.5MM)	2
9	R32-LCD32T-LG11	32"液晶屏LC320WXN-SBD1	1
8	54-L32010-244	L3201开关支架	1
7	82-L3201E-PKY01	L3201-S9 VDE电源开关组件(II类)	1
6	54-L32010-070	L3201电源钮	1
5	82-3201S9-FBY	L3201-S9控制板组件(带屏蔽)	1
4	82-3201S9-IRY	L3201-S9接收板组件(单红灯)	1
3	54-L32010-160	L3201导光柱	1
2	54-L32050-170	L3205装饰条	1
1	52-0L3205-100	L3205前座	1

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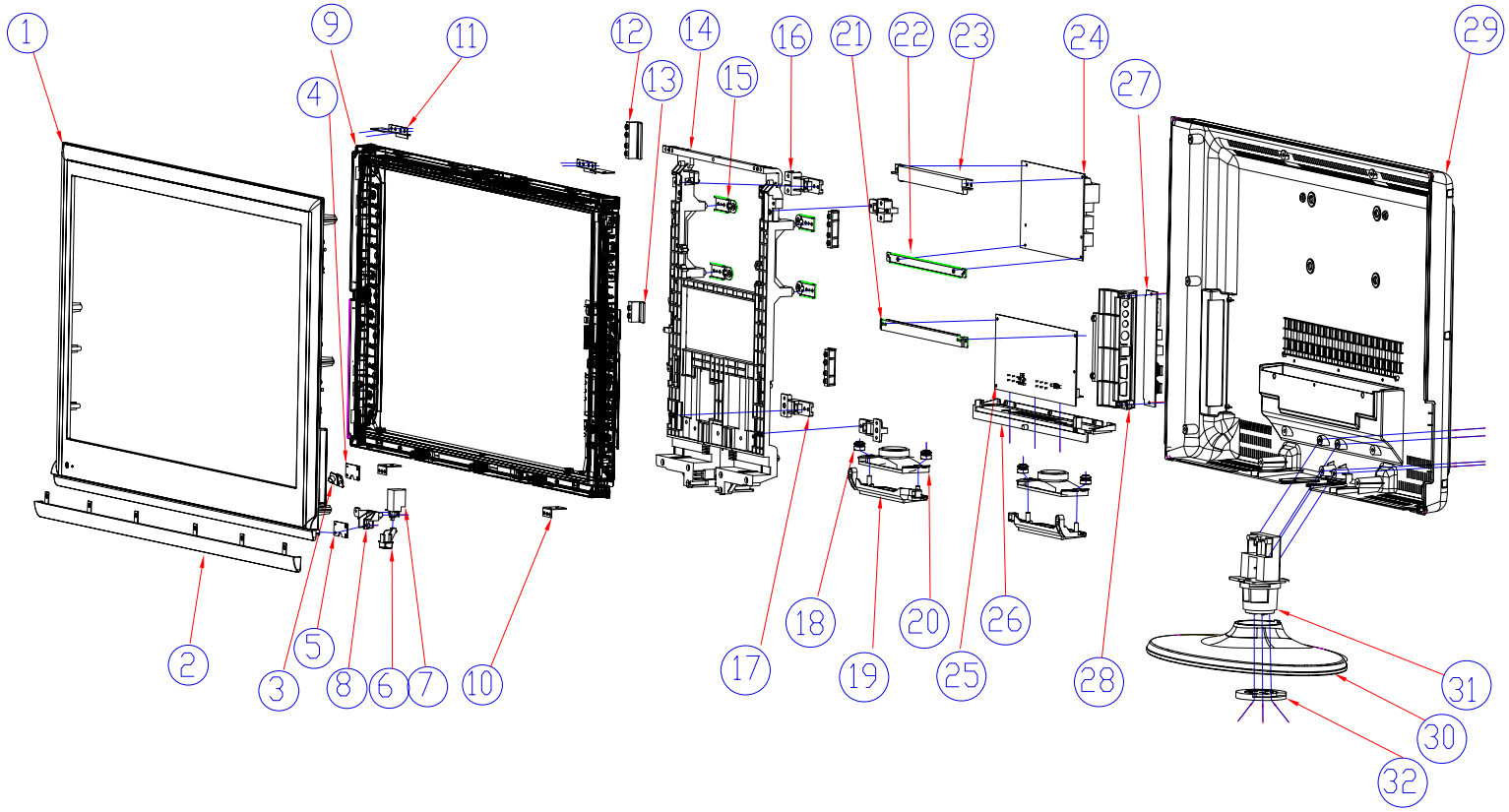
设 计			零件名称:	3205爆炸图	产品型号:		
审 核			物料编号:				
标准化			材 料:		单位	mm	比 例	
核准			表面处理:		数量		质 量	
公 差	0 ~ 30	±0.10	>30~100	±0.20	第 张 共 张			
	>100	±0.30	ANGULAR:	± 0.3°				
A2	3rd ANGLE PROJECTION				JPE 珠海经济特区金品电器有限公司			

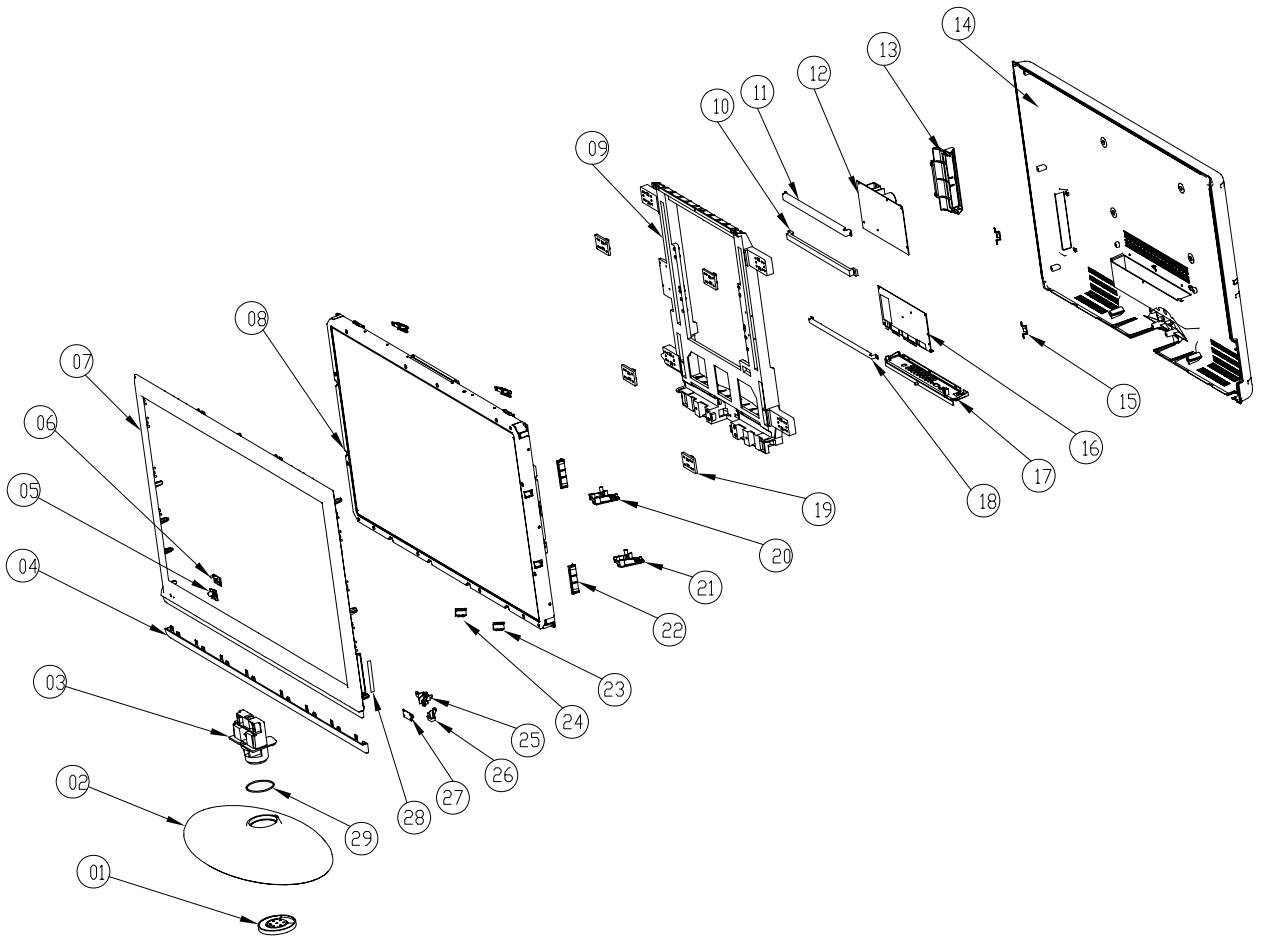
版本	区域	内容/描述	日期	签名
1		3701爆炸图		卢权均



序号	物料编号	名称	数量
32	54-L42010-270	4201法兰盘	1
31	54-L42010-260	4201转轴	1
30	54-L32010-110	底4201座	1
29	52-0L3701-300	3701后盖	1
28	54-L32010-242	侧AV支架	1
27	82-L320S9-AVY	L3201-S9 Side AVIN+USB组件	1
26	54-L3201S-020	端子板	1
25	82-L42PS9-MAY01	机芯板	1
24	R41-PDWHDZ-205	电源板	1
23	54-L32010-240	电源板支架	1
22	59-L3201R-0G01	电源板支撑铁条	1
21	59-L3201R-0G02	机芯板支撑铁条	1
20	82-3701L4-LB01	喇叭	1
19	54-L3201L-240	喇叭支架	1
18	55-100550-000	喇叭胶垫	4
17	54-L37010-251	3701连屏件	2
16	54-L37010-250	3701连屏件	2
15	59-L4201U-1G01	壁挂支架	4
14	54-L37010-010	3701主支架	1
13	54-L5501S-251	压屏件	2
12	54-L42010-252	4201压屏件	3
11	59-L3701W-0G03	压屏件	1
10	59-L3201P-0G02	侧锁件	2
9	R32-LCD32T-LG11	液晶屏	1
8	54-L32010-244	开关支架	1
7	82-3701L4-PKY01	电源开关	1
6	54-L32010-070	电源钮	1
5	82-3702M2-FBY	控制板	1
4	82-3701L4-IRY	接收板	1
3	54-L32010-160	导光柱	1
2	54-L37010-170	3701装饰条	1
1	52-0L3701-100	3701前座	1

设 计	卢权均		零件名称:	3701爆炸图	产品型号:	
审 核			物料编号:			
标准化			材 料:		单位 mm	比 例
核准			表面处理:		数量	质 量
公 差	0 ~ 30 ±0.10		>30~100 ±0.20		第 张 共 张	
	>100 ±0.30		ANGULAR: ± 0.3°		JPE 珠海经济特区金品电器有限公司	
A2	3rd ANGLE PROJECTION					

版本	区域	内容/描述	日期	签名



序号.	物料编码	物料名称	数量
30			
29		PVC 胶片	1
28	63-0L3201-B001	薄膜按键(E) 113.7*10mm,B/S	1
27	28-G00184-0010	按键PCB板	1
26	54-L32010-070	L3201电源组	1
25	54-L32010-244	L3201 电源开关支架	1
24	59-L4201W-1K02	压屏件 L4201W-0K01	1
23	59-L4201W-0K04	压屏件L4201W-0K02	3
22	54-L42010-252	L4201压屏件	5
21	54-L4201R-240	L4201(R) 喇叭支架 (R)	1
20	54-L4201L-240	L4201(L) 喇叭支架 (L)	1
19	54-L42010-250	L4201连屏垫	4
18	59-L4201R-0G02	L4201机芯支撑	1
17	54-L3201L-020	L3201(L4)端子板	1
16	82-L32KL4-May03	机芯板(L4)	4
15	59-L4201U-0G01	L4201壁挂支撑	1
14	52-0L4201-300	L4201后盖	1
13	54-L32010-241	L3201侧AV支架(L4)	1
12	82-L42T19-DY03	电源板(2804)	1
11	59-L4201R-0G01	L4201电源板支撑	1
10	54-L42010-240	L4201电源板支架	1
9	54-L42010-010	L4201主支架	1
8	82-L420S9-PP01	42 液晶屏	1
7	52-0L4201-100	L4201前框	1
6	82-3201S9-IRY	L3201-S9接收板	1
5	54-L32010-160	L3201导光柱	1
4	54-L42010-170	L4201装饰条	1
3	54-L42010-260	L4201转轴	1
2	54-L42010-110	L4201底座	1
1	54-L42010-270	L4201法兰盖	1

设 计	陈 志 江		零件名称:		产品型号:	L4201	
审 核			物料编号:				
标准化			材 料:		单位	mm	比 例	
核准			表面处理:		数量		质 量	
公 差	0 ~ 30	±0.10	>30~100	±0.20	第 张 共 张		
	>100	±0.30	ANGULAR:	± 0.3°	JPE 东海经济特区金品电器有限公司		
A2	3rd ANGLE PROJECTION						

MSTAR TSUMV36KU (SD)机芯软件升级说明

软件升级

一、准备

1. 准备SD机芯升级工具，升级工具是一头并口，一头是VGA口（如图1所示）。

图1

2.连接升级工具并口端到电脑主机并口端，连接升级VGA口到机芯板VGA插座，确认以上连接无误后打开液晶电视开关（如图2所示）。

注：此系列液晶电视具有关机记忆功能。如果上次关闭电源开关之前是使用遥控先待机，则再次打开电源开关后，也要使用遥控开机。升级之前液晶电视机一定要处于开机状态（指示灯不亮），不能处于待机状态（指示灯亮红色）。

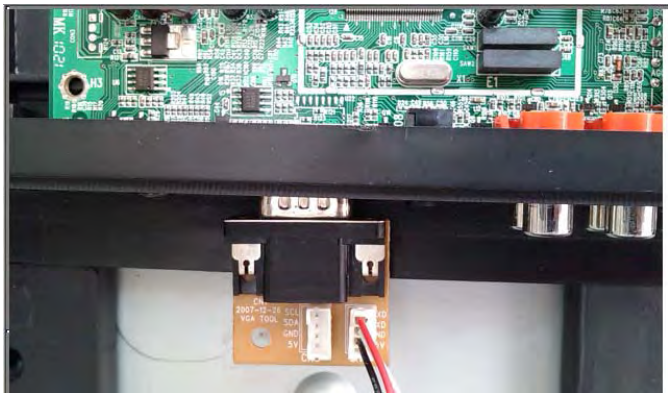


图2

二、软件升级

1.释放包裹文件ISP_Tool(SD).rar里面的程序文件ISP_Tool.exe到桌面。

图3

2，双击桌面ISP_Tool.exe，打开程序运行界面（如图4所示）。

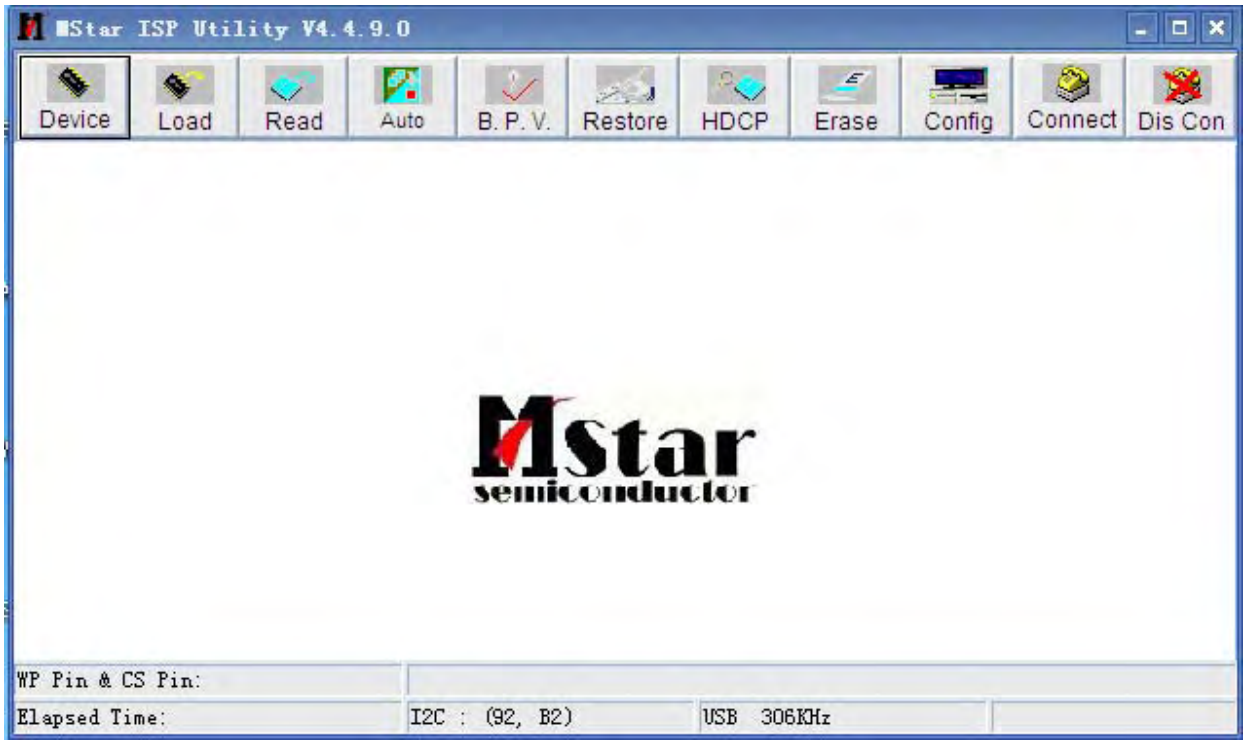


图4

3. 单击Config按钮 

，打开Config对话框，设置升级工具配置选项。

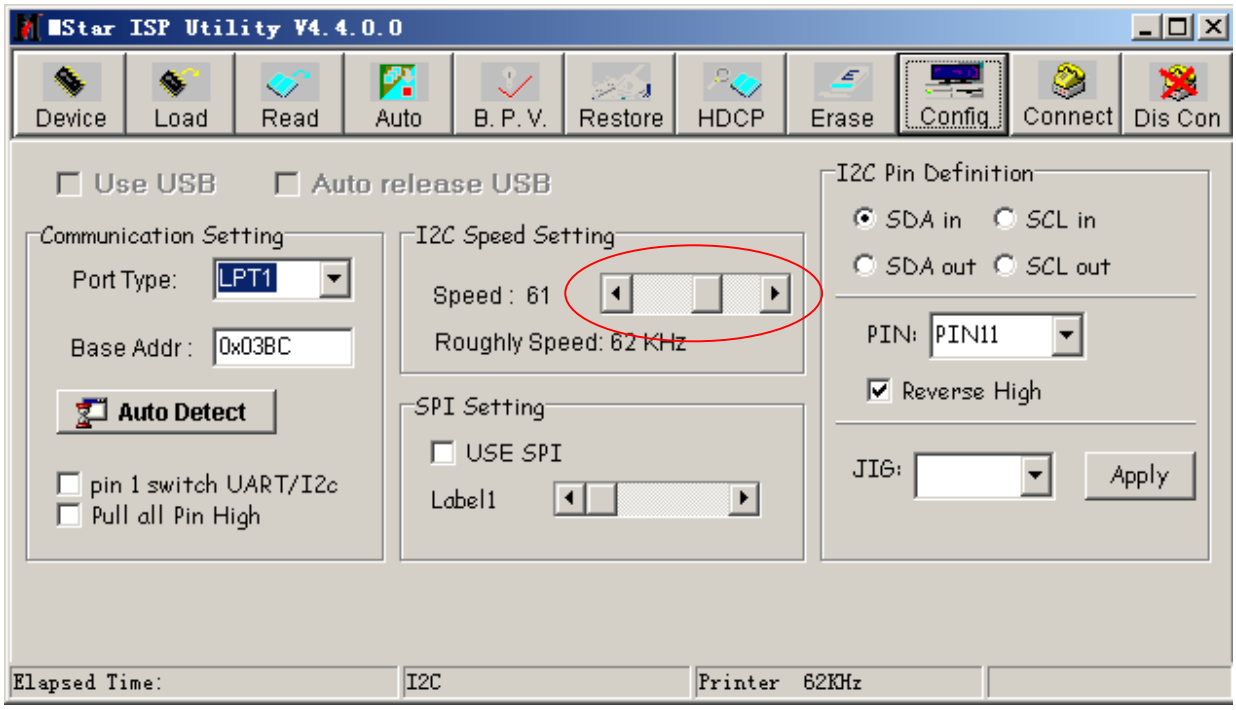


图5

1） 可根据电脑配置适当调节I2C Speed Setting来增加升级速度。

4. 单击Connect按钮 

，建立电脑与机芯板通信。

1) 如果连接成功则弹出如Isp_tool对话框，显示驱动类型为AT26DF081A

2) 如果连接失败，则弹出Dialog对话框，显示“can’t Find the Device Type!!”。连接失败是因为机芯板主芯片与flash没有工作，或者双方没有通信而引起。故障排除后重新连接直到成功。

图6

图7

5. 单击Read按钮 

，打开Read对话框。

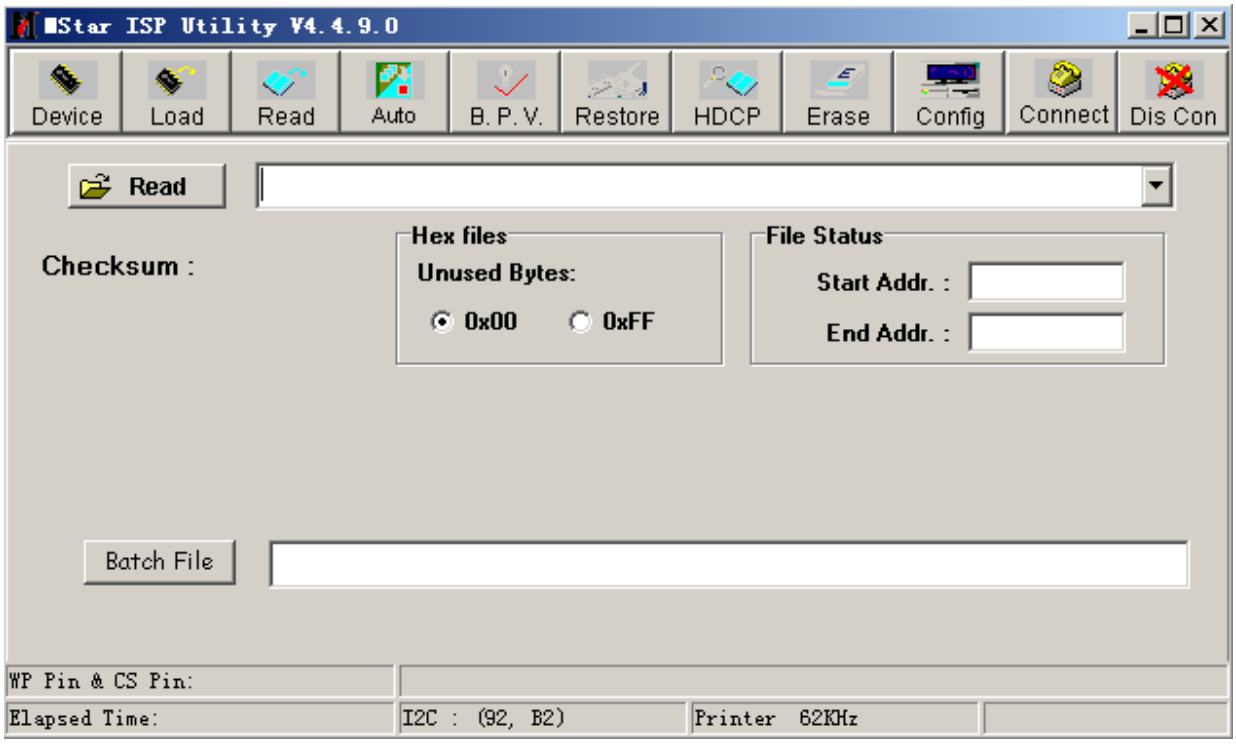


图8

1)，单击 

按钮，弹出打开对话框，选择升级文件(bin尾缀)，单击 

按钮，升级文件载入并返回主程序对话框。

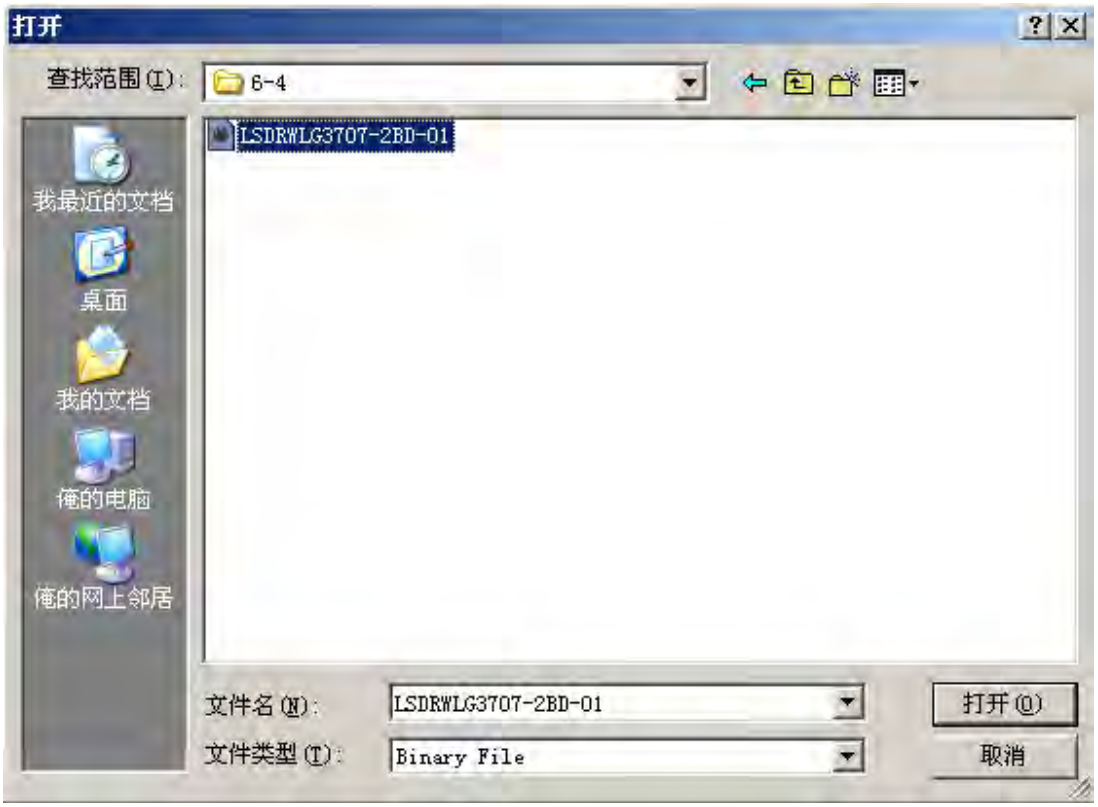


图9

6. 单击Auto按钮  ，打开Auto对话框。

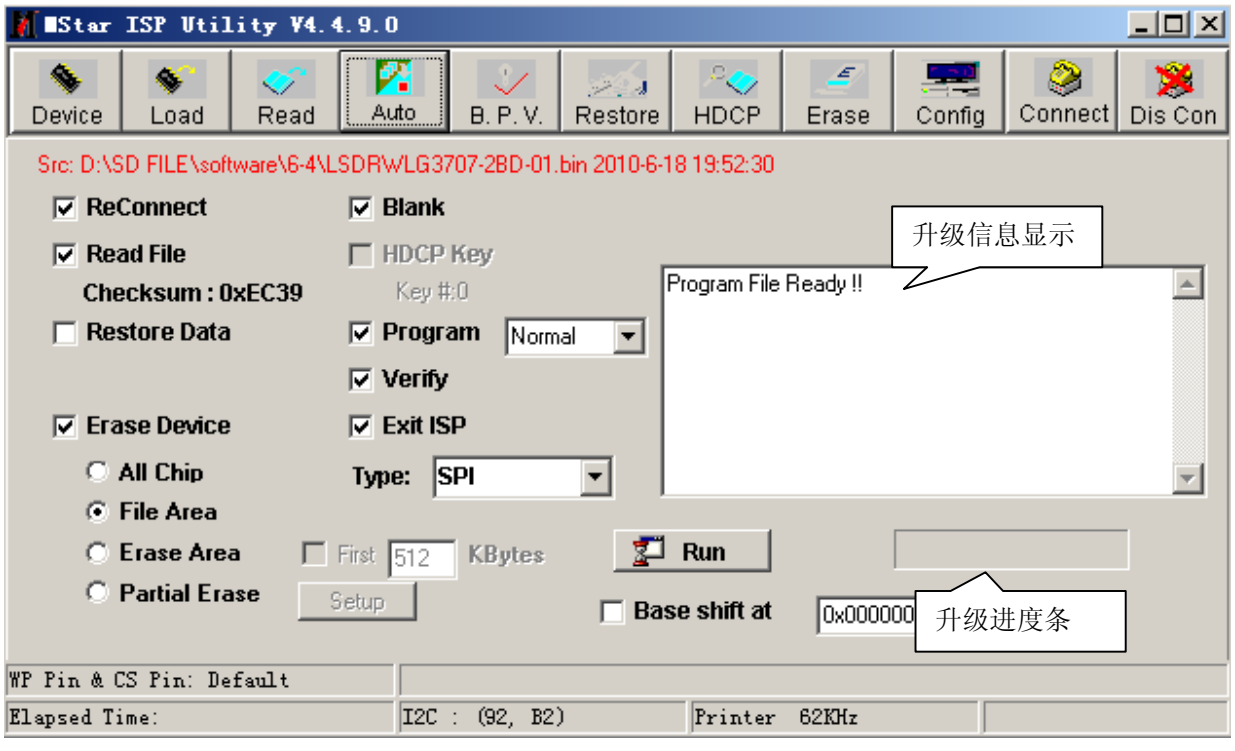


图10

1）Blank、Program、Verify、Exit ISP建议全部选中。

2）单击 Run 按钮开始升级。

升级中：

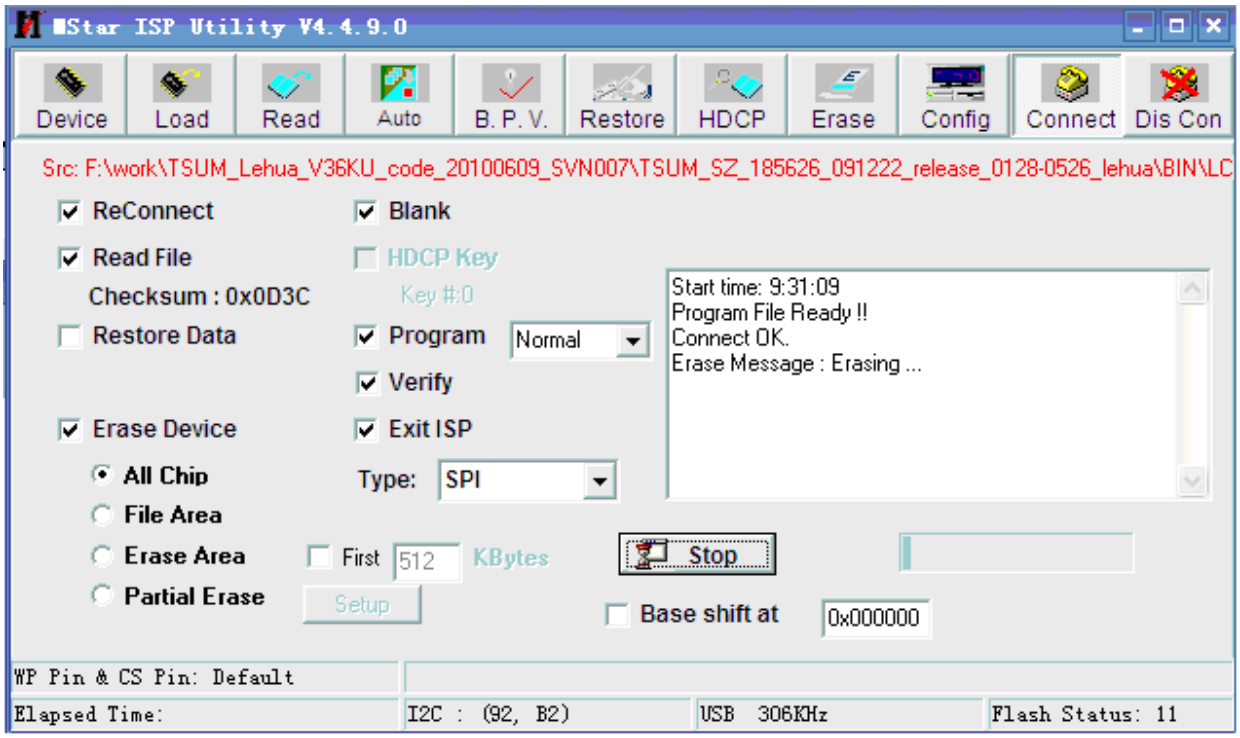
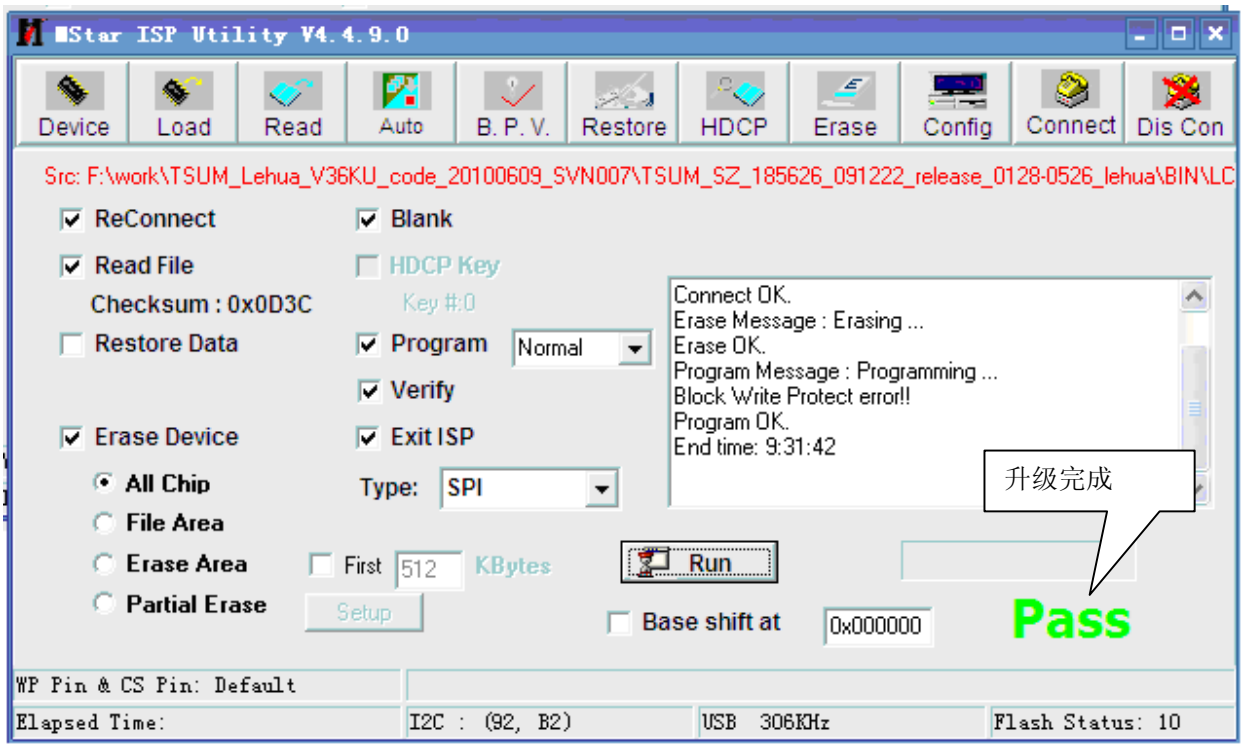


图11

3）升级完成后在升级进度条后面显示PAAS



4）软件升级完成后，将电视机电源开关关闭，等待指示灯从亮变为暗后（型号不一样，时间不等）约有30S，从新打开电源开关。

7.复位与检查

1）软件升级完成从新开机后，进入工厂模式（图12），按遥控器选择并进入“E2P ADJUST”子菜单（图13），选中“DEFAULT”项目，按遥控器左软键开始复位。复位过程中屏幕左上角显示“DEFAULT”（图14）。当“DEFAULT”自动显示后并进入TV模式，复位完成。

进入工厂模式方法：按遥控器“图像模式”键，再连按数字键“5”“8”“0”即可进入工厂调试菜单。按遥控器“菜单”键可以退出工厂调试模式。

2）进入工厂调试菜单检查软件版本是否正确

进入工厂模式后，在工厂菜单最下方显示的是软件本版号。

图12 工厂菜单

图13 E2P ADJUST 子菜单，

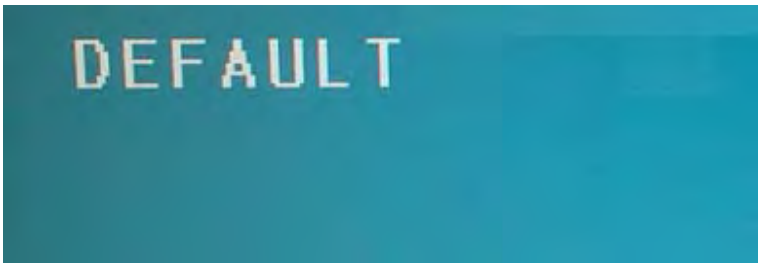


图13 复位过程中，显示EDFAULT

8.升级完成