AK56

SERVICE MANUAL

SERVICE MANUEL
for
11AK56

Date : **16/01/2007**

Version : **1**

Status : **Draft**

Unit : **Electronic Hardware Design**

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	16/01/2007		Draft	YALÇIN ELİK	SERDAR GÜLTEN

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1. Introduction

1.1. Purpose

This document is prepared for the UOCII TV project and describes the whole system features and operating principles to be used in hardware design phase.

The document is based on "Device Specification UOCII-Version 1.12" from **Philips Semiconductors**.

Prior to hardware design start, all parties involved must agree with the contents of this document.

1.2. Scope

The document covers detailed descriptions of 11AK56 chassis system building blocks.

1.3. General Features

11AK56 is a 90° / 50 Hz. chassis which is capable of driving 14"/20" superflat and 15" realflat CRT's .

The chassis will have the following main features;

- Remote Control
- 100 programs
- On Screen Display
- Mono
- Colour Standarts ; PAL, SECAM, NTSC,
- Transmission standarts ; B/G, L/L' I/I', DK,
- Teletext ; One pages or Seven Page
- Multi-standard alignment free PLL tuning,
- Europe Scart or Back AV input
- Detachable headphone output option,
- Front or side or AV input option,
- Back AV output option,
- 2W (%10 THD),
- 90-270V 50Hz or 170V-270V 50Hz SMPS
- Less than 3W or Less than 5W

2. General Description

2.1. Introduction

This chapter describes system building blocks and their detailed descriptions.

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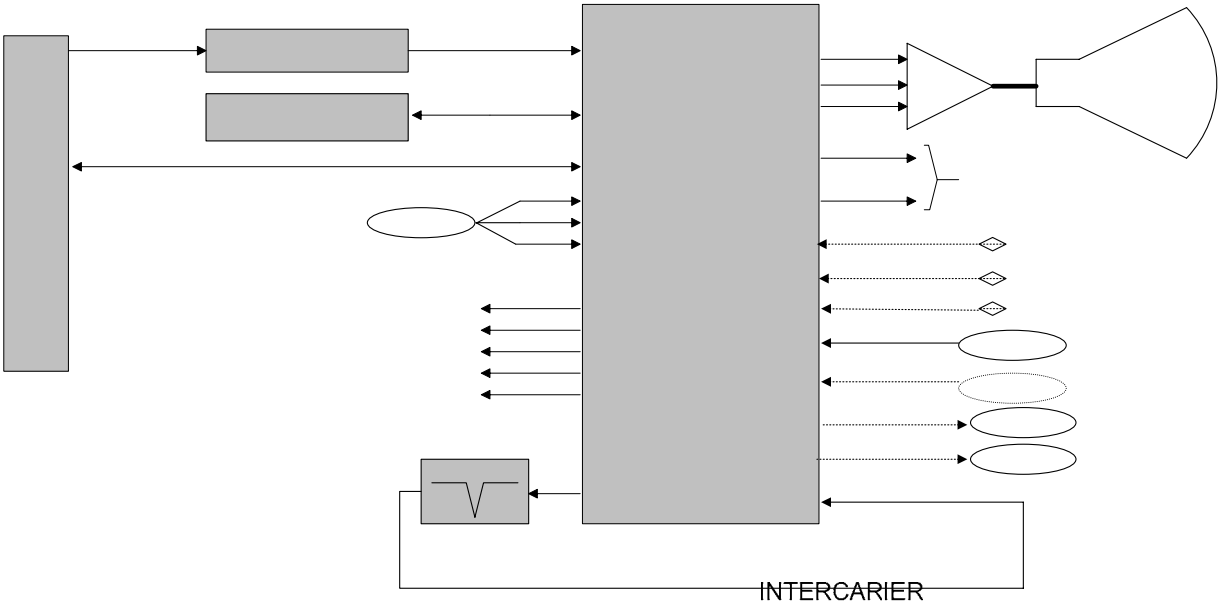
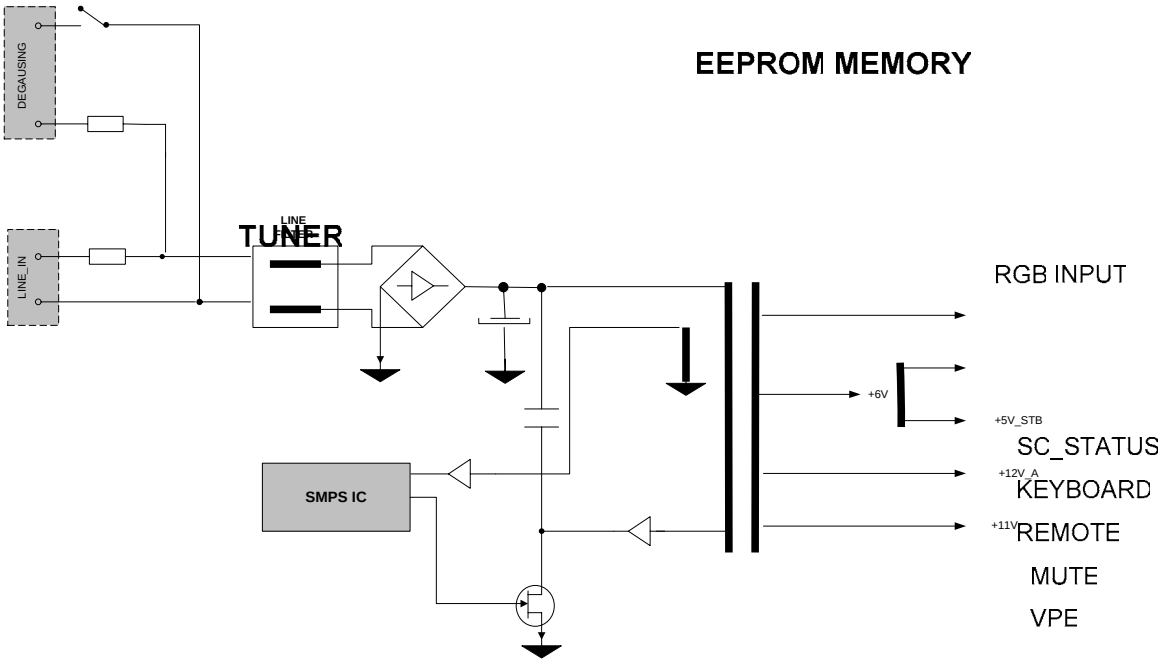
2.2. System Building Blocks

2.2.1. AK57 Chassis Block Diagrams

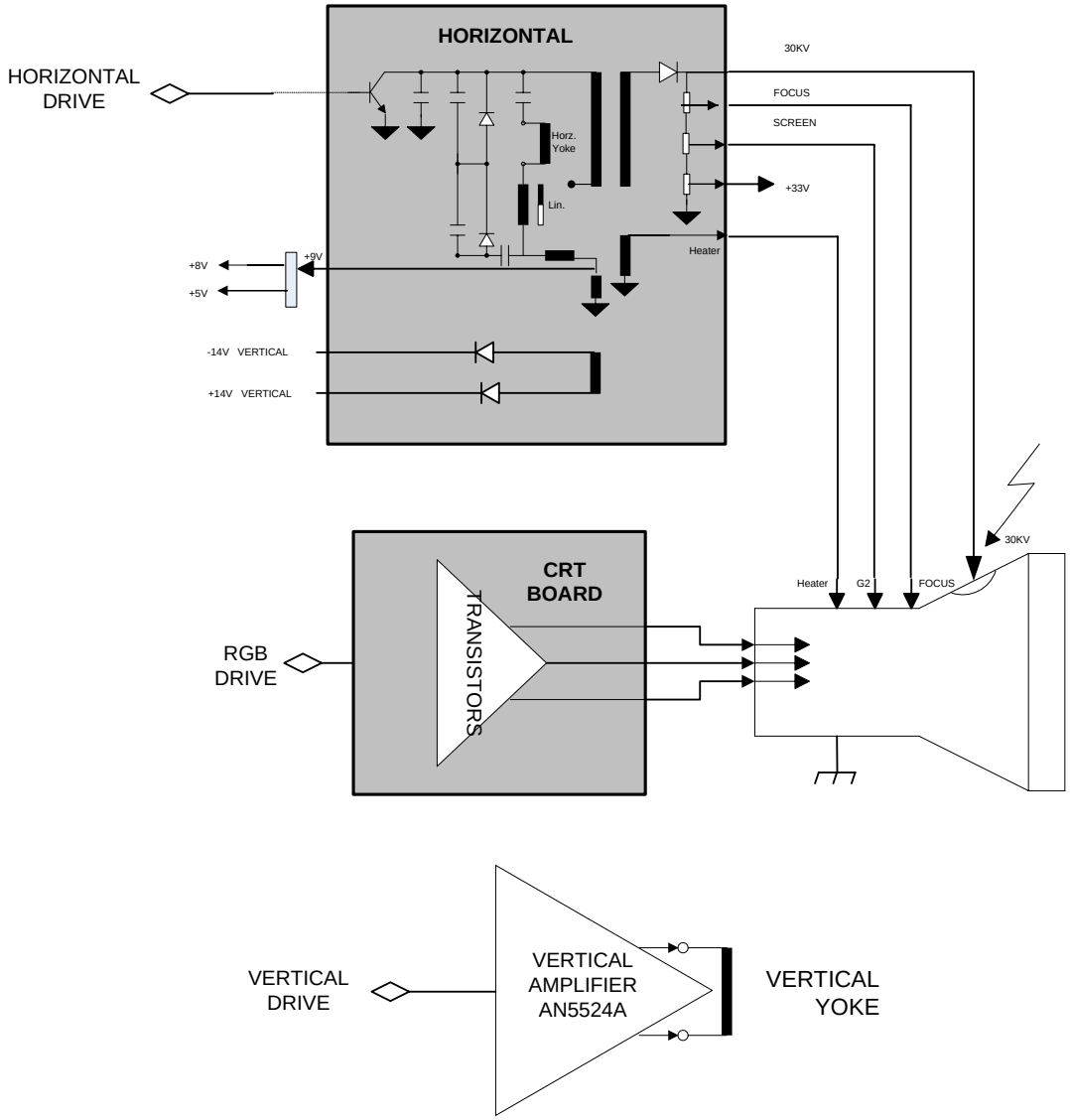
2.2.1.1. Genaral



2.2.1.2. SMPS



2.2.1.3. DEFLECTION



2.2.2. AK56 Chassis Main Blocks

AK57 chassis main blocks are;

- **UOC11** : Microcontroller + Video Proccessor + Sound Proccessor + IF + Teletext

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- **AUDIO** : Audio Amp.,
- **EXT. AV I/O** : Scart , AV input, AV output,
- **TUNER** : PLL Tuner
- **SAW FILTERS**
- **SMPS** : SMPS Controller, SMT, Bridge Rect., Line Filters
- **DEFLECTION** : FBT, HOT, Vertical Amplifier, Line Driver,
- **CRT BOARD** : RGB Amp. with transistors,

2.2.2.1. UOC-II (ULTIMATE-ONE-CHIP)

UOCII is composed of microcontroller, video proccessor, sound proccessor and IF blocks.

The various versions of the TDA955X H/N1 series combine the functions of a video processor together with a microcontroller.The ICs are intended to be used in economy television receivers with 90 and 110 degree picture tubes.

The ICs have supply voltages of 8V and 3.3V and they are mounted in a QFP 80 envelope.

The features are given in the following feature list.

FEATURES

TV-signal processor

- Multi-standard vision IF circuit with alignment-free PLL demodulator
- Internal (switchable) time-constant for the IF-AGC circuit
- The QSS and mono FM functionality are both available so that an FM/AM TV receiver can be built without the use of additional ICs
- The mono intercarrier sound circuit has a selective
- FM-PLL demodulator which can be switched to the different FM sound frequencies (4.5/5.5/6.0/6.5 MHz). The quality of this system is such that the external band-pass filters can be omitted.
- The FM-PLL demodulator can be set to centre frequencies of 4.74/5.74 MHz so that a second sound channel can be demodulated. In such an application it is necessary that an external bandpass filter is inserted.
- The vision IF and mono intercarrier sound circuit can be used for the demodulation of FM radio signals
- Video switch with 2 external CVBS inputs and a CVBS output. One of the CVBS inputs can be used as Y/C input.
- 2 external audio inputs. The selection of the various inputs is coupled to the selection of the CVBS signals
- Integrated chrominance trap circuit
- Integrated luminance delay line with adjustable delay time
- Switchable group delay correction in the CVBS path
- Picture improvement features with peaking (with switchable centre frequency, depeaking, variable positive/negative overshoot ratio and video dependent coring), dynamic skin tone control and blue-, black- and white stretching
- Integrated chroma band-pass filter with switchable centre frequency

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- Switchable DC transfer ratio for the luminance signal
- Only one reference (12 MHz) crystal required for the m-Controller, Teletext- and the colour decoder
- PAL/NTSC or multi-standard colour decoder with automatic search system
- Internal base-band delay line
- Indication of the Signal-to-Noise ratio of the incoming CVBS signal
- A linear RGB/YUV/YPBPR input with fast blanking for external RGB/YUV sources. The synchronisation circuit can be connected to the incoming Y signal. The Text/OSD signals are internally supplied from the
- m-Controller/Teletext decoder.
- RGB control circuit with 'Continuous Cathode Calibration', white point and black level off-set adjustment so that the colour temperature of the dark and the light parts of the screen can be chosen independently.
- Contrast reduction possibility during mixed-mode of OSD and Text signals
- Adjustable 'wide blanking' of the RGB outputs
- Horizontal synchronization with two control loops and alignment-free horizontal oscillator
- Vertical count-down circuit
- Vertical driver optimized for DC-coupled vertical output stages
- Horizontal and vertical geometry processing
- Horizontal and vertical zoom function for 16 : 9 applications
- Horizontal parallelogram and bow correction for large screen picture tubes
- Low-power start-up of the horizontal drive circuit

Microcontroller

- 80C51 m-controller core standard instruction set and timing
- 1 ms machine cycle
- 32 - 128Kx8-bit late programmed ROM
- 3 - 12Kx8-bit DataRAM (shared between Display, Acquisition and Auxiliary RAM)
- Interrupt controller for individual enable/disable with two level priority
- Two 16-bit Timer/Counter registers
- One 16-bit Timer with 8-bit Pre-scaler
- WatchDog timer
- Auxiliary RAM page pointer
- 16-bit Data pointer
- Stand-by, Idle and Power Down modes
- 14 bits PWM for Voltage Synthesis Tuning
- 8-bit A/D converter with 4 multiplexed inputs
- 5 PWM (6-bits) outputs for control of TV analogue signals
- 18 general I/O ports

Data Capture

- Text memory for 1 or 10 pages
- In the 10 page versions inventory of transmitted Teletext pages stored in the Transmitted Page Table (TPT) and Subtitle Page Table (SPT)
- Data Capture for US Closed Caption

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- Data Capture for 525/625 line WST, VPS (PDC system A) and Wide Screen Signalling (WSS) bit decoding
- Automatic selection between 525 WST/625 WST
- Automatic selection between 625 WST/VPS on line 16 of VBI
- Real-time capture and decoding for WST Teletext in Hardware, to enable optimized m-processor throughput
- Automatic detection of FASTEXT transmission
- Real-time packet 26 engine in Hardware for processing accented, G2 and G3 characters
- Signal quality detector for video and WST/VPS data types
- Comprehensive teletext language coverage
- Full Field and Vertical Blanking Interval (VBI) data capture of WST data

Display

- Teletext and Enhanced OSD modes
- Features of level 1.5 WST and US Close Caption
- Serial and Parallel Display Attributes
- Single/Double/Quadruple Width and Height for characters
- Scrolling of display region
- Variable flash rate controlled by software
- Enhanced display features including overlining, underlining and italics
- Soft colours using CLUT with 4096 colour palette
- Globally selectable scan lines per row (9/10/13/16) and character matrix [12x10, 12x13, 12x16 (VxH)]
- Fringing (Shadow) selectable from N-S-E-W direction
- Fringe colour selectable
- Meshing of defined area
- Contrast reduction of defined area
- Cursor
- Special Graphics Characters with two planes, allowing four colours per character
- 32 software redefinable On-Screen display characters
- 4 WST Character sets (G0/G2) in single device (e.g. Latin, Cyrillic, Greek, Arabic)
- G1 Mosaic graphics, Limited G3 Line drawing characters
- WST Character sets and Closed Caption Character set in single device

Optional Used ICs at AK57 chassis are TDA9550 H/N1, TDA9551 H/N1, TDA9552 H/N1.

FUNCTIONALOF TDA9550 H/N1

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch
- Automatic Volume Levelling
- PAL decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext

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- Close Captioning

FUNCTIONALOF TDA9551H

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch
- Automatic Volume Levelling
- PAL decoder
- SECAM decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext
- Close Captioning

FUNCTIONALOF TDA9552H

- TV range is 90°
- Mono intercarrier multi-standard sound demodulator (4.5 - 6.5 MHz) with switchable centre frequency Audio switch
- Automatic Volume Levelling
- QSS sound IF amplifier with separate input and AGC circuit
- AM sound demodulator without extra reference circuit
- PAL decoder
- SECAM decoder
- NTSC decoder
- ROM size 32 – 64K
- User RAM size 1K
- One page teletext
- Close Captioning

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QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Supply					
V_P	supply voltages	–	8.0/3.3	–	V
I_P	supply current (V_P = 8 V)	–	135	–	mA
I_P	supply current (V_P = 3.3 V)	–	60	–	mA
Input voltages					
$V_{iVIFrms)}$	video IF amplifier sensitivity (RMS value)	–	75	–	µV
$V_{iSIF(rms)}$	QSS sound IF amplifier sensitivity (RMS value)	–	60	–	µV
$V_{iAUDIO(rms)}$	external audio input (RMS value)	–	500	–	mV
$V_{iCVBS(p-p)}$	external CVBS/Y input (peak-to-peak value)	–	1.0	–	V
$V_{iCHROMA(p-p)}$	external chroma input voltage (burst amplitude) (peak-to-peak value)	–	0.3	–	V
$V_{iRGB(p-p)}$	RGB inputs (peak-to-peak value)	–	0.7	–	V
$V_{iY(p-p)}$	luminance input signal (peak-to-peak value)	–	1.4 / 1.0	–	V
$V_{iU(p-p)}$ / $V_{iPB(p-p)}$	U / P_B input signal (peak-to-peak value)	–	–1.33 / +0.7	–	V
$V_{iV(p-p)}$ / $V_{iPR(p-p)}$	V / P_R input signal (peak-to-peak value)	–	–1.05 / +0.7	–	V
Output signals					
$V_{o(IFVO)(p-p)}$	demodulated CVBS output (peak-to-peak value)	–	2.0	–	V
$V_{o(QSSO)(rms)}$	sound IF intercarrier output in QSS versions (RMS value)	–	100	–	mV
$V_{o(AMOUT)(rms)}$	demodulated AM sound output in QSS versions (RMS value)	–	500	–	mV
$V_{o(CVBSO)(p-p)}$	selected CVBS output (peak-to-peak value)	–	2.0	–	V
$I_{o(AGCOUT)}$	tuner AGC output current range	0	–	5	mA
$V_{oRGB(p-p)}$	RGB output signal amplitudes (peak-to-peak value)	–	2.0	–	V
I_{oHOUT}	horizontal output current	10	–	–	mA
I_{oVERT}	vertical output current (peak-to-peak value)	1	–	–	mA
I_{oEWD}	EW drive output current	1.2	–	–	mA

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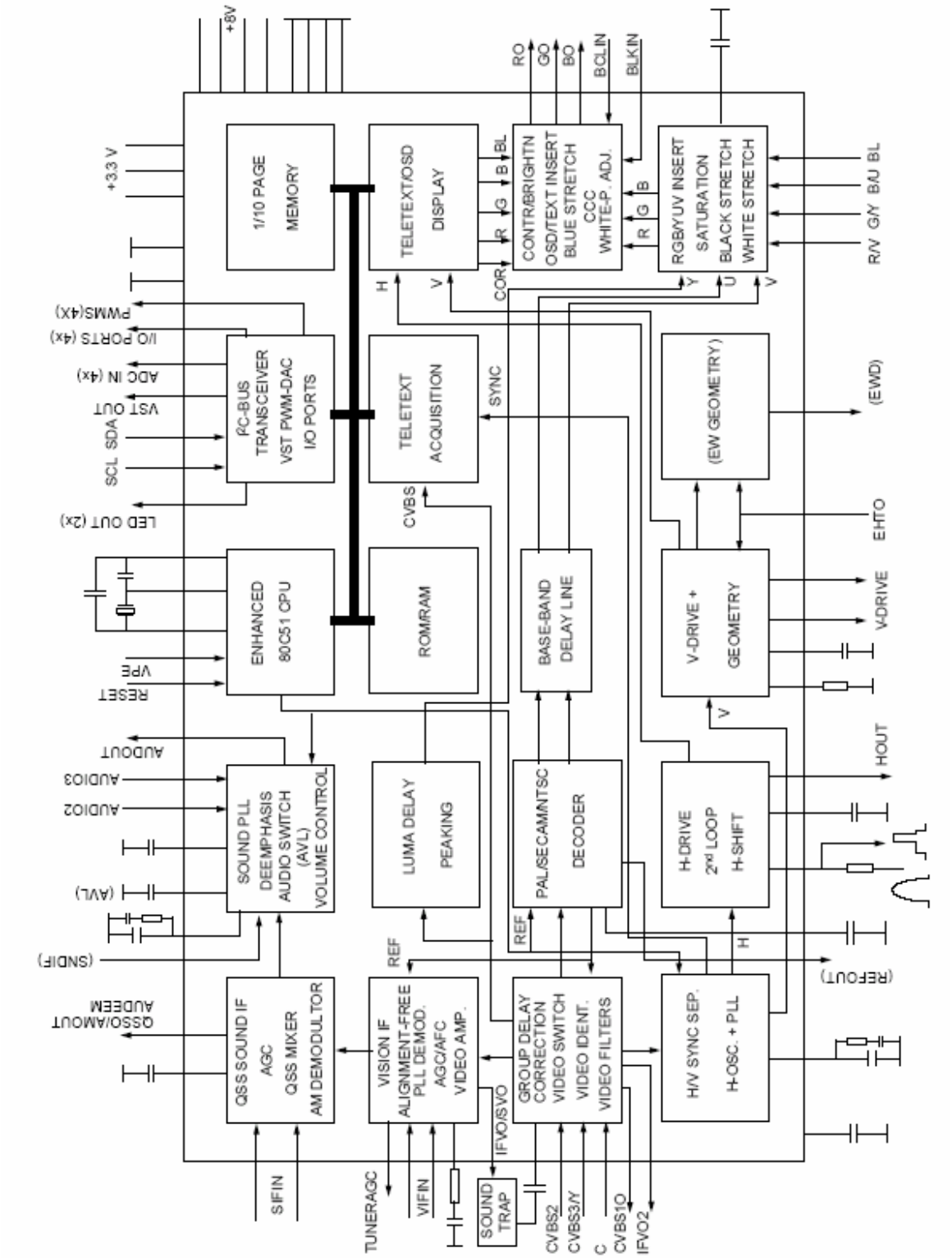
BLOCK DIAGRAM



PINING

SYMBOL	PIN	DESCRIPTION
P3.1/ADC1	1	port 3.1 or ADC1 input
P3.2/ADC2	2	port 3.2 or ADC2 input
P3.3/ADC3	3	port 3.3 or ADC3 input
VSSC/P	4	digital ground for µ-Controller core and periphery
P0.5	5	port 0.5 (8 mA current sinking capability for direct drive of LEDs)
P0.6/CVBSTD	6	port 0.6 (8 mA current sinking capability for direct drive of LEDs) or Composite video input. A positive-going 1V(peak-to-peak) input is required
VSSA	7	analog ground of Teletext decoder and digital ground of TV-processor
SECPLL	8	SECAM PLL decoupling
VP2	9	2nd supply voltage TV-processor (+8 V)
DECDIG	10	supply voltage decoupling of digital circuit of TV-processor
PH2LF	11	phase-2 filter
PH1LF	12	phase-1 filter
GND3	13	ground 3 for TV-processor
DECBG	14	bandgap decoupling
AVL/EWD (1)	15	Automatic Volume Levelling (90° versions) / E-W drive output (110° versions)
VDRB	16	vertical drive B output
VDRA	17	vertical drive A output
IFIN1	18	IF input 1
IFIN2	19	IF input 2
IREF	20	reference current input
VSC	21	vertical sawtooth capacitor
AGCOUT	22	tuner AGC output
SIFIN1	23	SIF input 1
SIFIN2	24	SIF input 2
GND2	25	ground 2 for TV processor
SNDPLL	26	narrow band PLL filter
AVL/REF0/SNDIF (1)	27	Automatic Volume Levelling / subcarrier reference output / sound IF input
AUDIO2	28	audio 2 input
AUDIO3	29	audio 3 input
HOUT	30	horizontal output
FBISO	31	flyback input/sandcastle output
DECSDEM	32	decoupling sound demodulator
QSSO/AMOUT/ AUDEEM (1)	33	QSS intercarrier output / AM output in stereo applications or deemphasis (front-end audio out) / AM output in mono applications
EHTO	34	EHT/overvoltage protection input
PLLIF	35	IF-PLL loop filter
SIFAGC	36	AGC sound IF
QSSO	37	QSS output
IFVO/SVO	38	IF video output / selected CVBS output
VP1	39	main supply voltage TV processor
CVBS1	40	internal CVBS input
GND	41	ground for TV processor
CVBS2	42	external CVBS2 input

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SYMBOL	PIN	DESCRIPTION
GND	43	ground for TV-processor
CVBS3/Y	44	CVBS3/Y input
C	45	chroma input
WHSTR	46	white stretch capacitor
CVBSO	47	CVBS output
AUDOUT /AMOUT(1)	48	audio output /AM audio output (volume controlled)
IFVO2	49	2nd IF video output signal (with or without group delay correction)
INSSW2	50	2nd RGB / YUV insertion input
R2/VIN	51	2nd R input / V (R-Y) input / P_R input
G2/YIN	52	2nd G input / Y input
B2/UIN	53	2nd B input / U (B-Y) input / P_B input
BCLIN	54	beam current limiter input
BLKIN	55	black current input / V-guard input
RO	56	Red output
GO	57	Green output
BO	58	Blue output
VDDA	59	analog supply of Teletext decoder and digital supply of TV-processor (3.3 V)
VPE	60	OTP Programming Voltage
VDDC	61	digital supply to core (3.3 V)
OSCGND	62	oscillator ground supply
XTALIN	63	crystal oscillator input
XTALOUT	64	crystal oscillator output
RESET	65	reset
VDDP	66	digital supply to periphery (+3.3 V)
P1.0/INT1	67	port 1.0 or external interrupt 1 input
P1.1/T0	68	port 1.1 or Counter/Timer 0 input
P1.2/INT0	69	port 1.2 or external interrupt 0 input
P1.3/T1	70	port 1.3 or Counter/Timer 1 input
P1.6/SCL	71	port 1.6 or I^2C-bus clock line
P1.7/SDA	72	port 1.7 or I^2C-bus data line
P2.0/TPWM	73	port 2.0 or Tuning PWM output
P2.1/PWM0	74	port 2.1
P2.2/PWM1	75	port 2.2
P2.3/PWM2	76	port 2.3
P2.4/PWM3	77	port 2.4
P2.5/PWM4	78	port 2.5
SYNC_FILTER	79	CVBS (i.e. P0.6/CVBS) Sync filter input: This pin should be connected to V_{SSA} via a 100 nF capacitor.
P3.0/ADC0	80	port 3.0 or ADC0 input

Note

1. The function of pin 15, 27, 33 and 48 is dependent on the mode of operation (mono intercarrier mode / QSS IF amplifier and East-West output or not) and is controlled by some software control bits. The valid combinations are given in table 1.

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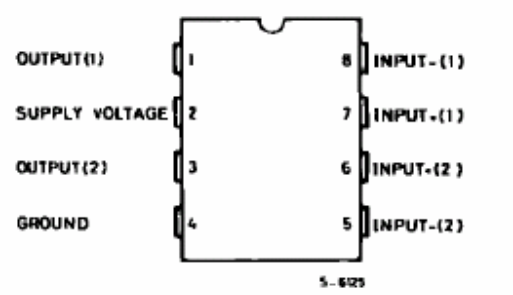
2.2.2.2. Audio

The TDA2822 is DUAL LOW-VOLTAGE POWER AMPLIFIER.

- Supply voltage down to 1.8V
- Low crossover distorsion
- Low qu escent current
- Bridge or stereo configuration



ELECTRICALCHARACTERISTICS

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_s	Supply Voltage		3		15	V
V_c	Quiescent Output Voltage	V_s = 9 V V_s = 6 V		4 2.7		V V
I_d	Quiescent Drain Current			6	12	mA
I_b	Input Bias Current			100		nA
P_o	Output Power (each channel)	d = 10 % f = 1 kHz V_s = 9 V R_L = 4 Ω V_s = 6 V R_L = 4 Ω V_s = 4.5 V R_L = 4 Ω	 1.3 0.45	 1.7 0.65 0.32		 W W W
G_v	Closed Loop Voltage Gain	f = 1 kHz	36	39	41	dB
R_i	Input Resistance	f = 1 kHz	100			kΩ
^eN	Total Input Noise	R_s = 10 kΩ B = 22 Hz to 22 kHz Curve A		2.5 2		µV µV
SVR	Supply Voltage Rejection	f = 100 Hz	24	30		dB
CS	Channel Separation	R_g = 10 kΩ f = 1 kHz		50		dB

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Figure: Test Circuit (Stereo)

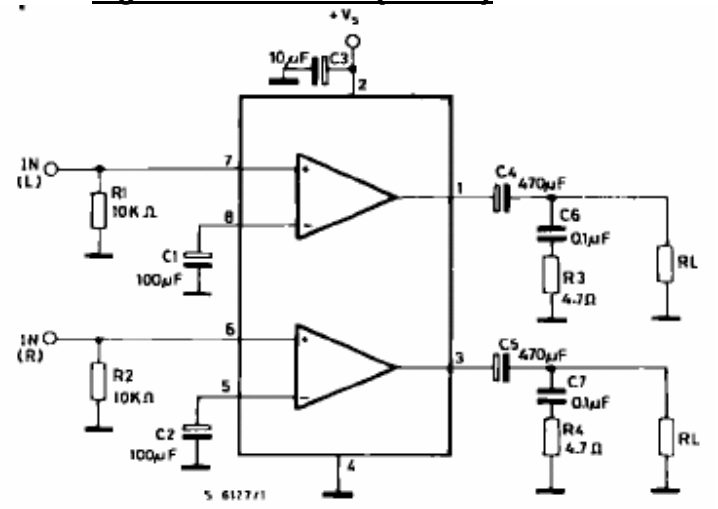

Figure: Test Circuit (Bridge)

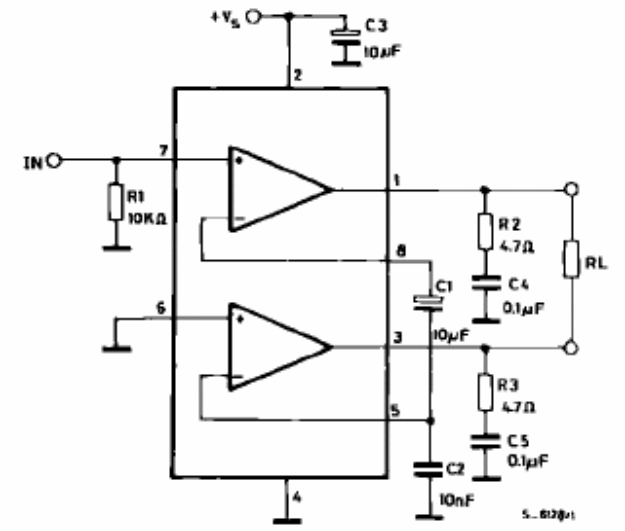

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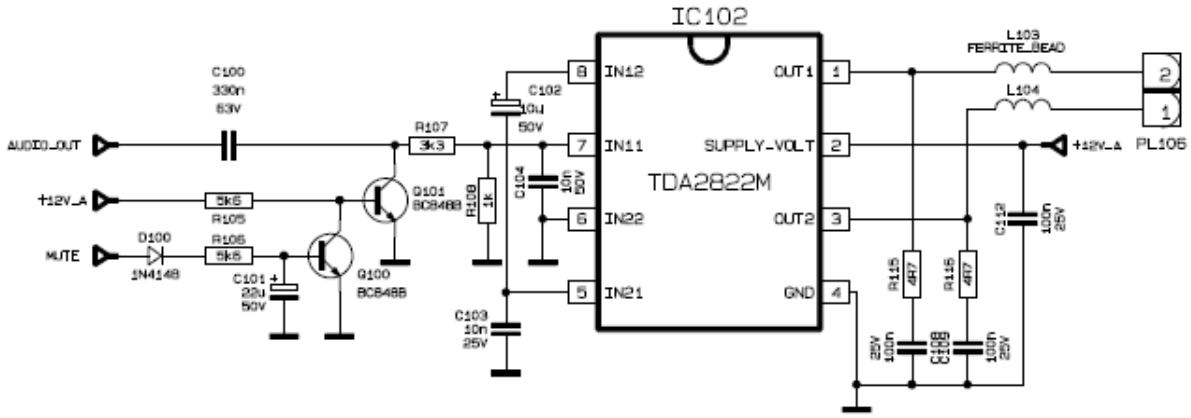
Figure: Application in 11AK56



2.2.2.3. External AV I/O

SCART PINING

1.	Audio right output	0.5Vrms / 1KΩ
2.	Audio right input	0.5Vrms / 10KΩ
3.	Audio left output	0.5Vrms / 1KΩ
4.	Ground AF	
5.	Ground Blue	
6.	Audio left input	0.5Vrms / 10KΩ
7.	Blue input	0.7Vpp / 75Ω
8.	AV switching input	0-12VDC /10KΩ
9.	Ground Green	
10.	Not Used	
11.	Green input	0.7Vpp / 75Ω
12.	Not Used	
13.	Ground Red	
14.	Ground Blanking	
15.	Red input	0.7Vpp / 75Ω
16.	Blanking input	0-0.4VDC, 1-3VDC / 75Ω
17.	Ground CVBS output	
18.	Ground CVBS input	
19.	CVBS output	1Vpp / 75Ω
20.	CVBS input	1Vpp / 75Ω
21.	Ground	

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Front/Side/Back AV Input

Audio 0.5Vrms / 10KΩ
Video 1Vpp / 75Ω

Back AV Output

Audio 0.5Vrms / 1KΩ
Video 1Vpp / 75Ω

2.2.2.4. TUNER

Channel coverage of PLLTuner for VHF/UHF

BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low Band	E2 to C	48.25 to 82.25 (1)	S01 to S08	69.25 to 154.25
Mid Band	E5 to E12	175.25 to 224.25	S09 to S38	161.25 to 439.25
High Band	E21 to E69	471.25 to 855.25 (2)	S39 to S41	447.25 to 463.25

(1). Enough margin is available to tune down to 45.25 MHz.
(2). Enough margin is available to tune up to 863.25 MHz.

Noise	Typical	Max.	**Gain**	Min.	Typical	Max.
Low band :	5dB	9dB	All channels	: 38dB	44dB	52dB
Mid band :	5dB	9dB	Gain Taper (of-air channels):			8dB
High band :	6dB	9dB				

Noise is typically 6dB for all channels. **Gain** is minimum 38dB and maximum 50dB for all channels.

Terminals for External Connection

NO	TERMINAL NAME	DESCRIPTION
1	AGC	AGC Voltage input
2	NC	No Internal connection
3	SAS	Serial Address Selection
4	SCL	Serial Clock Line
5	SDA	Serial Data Line
6	NC	No Internal connection
7	BP	B+ for Internal IC
8	ADC	Analog/Digital Converter input
9	BT	Tuning Voltage supply
10	IF2	IF output 2
11	IF1	IF output 1
12	ANT	VHF/UHF signal input
13	SUB P/J	VHF/UHF signal output for PIP sub-tuner.

Electrical conditions

PAR	DESCRIPTION	MIN	TYP	MAX	UNIT
V_{B+}	B+ Supply Voltage	4.75	5.0	5.5	V
I_{B+}	B+ Supply Current (LNA OFF)		85	120	mA
	B+ Supply Current (LNA ON)		125	160	mA
V_{AGC}	AGC Input Voltage		4.0	4.5	V
VT	Tuning Supply voltage	30	33	35	V
V_{RIPPLE}	Permissible ripple (20Hz to 500kHz)			5	mV_{P-P}
V_{SCL}	Serial clock input Voltage (see Note1)			5.5	V
V_{SDA}	Serial data input Voltage (see Note1)			5.5	V

2.2.2.5. SAW FILTERS

2.2.2.5.1. K3958M (IF Filter for Video Applications)

Standard

- B/G
- D/K
- I
- L/L'

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Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF video filter with Nyquist slopes at 33.90 MHz and 38.90 MHz
- Constant group delay

2.2.2.5.2. K9656M (IF Filter for Audio Applications)

Standard

- B/G
- D/K
- I
- L/L'

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF audio filter with two channels
- Channel 1 (L') with one pass band for sound carriers at 40,40 MHz (L') and 39,75 MHz (L'- NICAM)
- Channel 2 (B/G, D/K, L, I) with one pass band for sound carriers between 32,35 MHz and 33,40 MHz

2.2.2.5.3. K2966 (IF Filter for Intercarrier Applications)

Standard

- B/G
- D/K

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground

4 Output
5 Output

Features

- TV IF filter with Nyquist slope and sound shelf
- Broad sound shelf for sound carriers at 32,40MHz and 33,40 MHz
- Group delay predistortion

2.2.2.5.4. K2962 (IF Filter for Intercarrier Applications)

Standard

- B/G
- I
- L/L'

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF filter with two Nyquist slope and sound shelf
- Picture carriers at 33,90 MHz and 38,90 MHz
- Broad sound shelf at 15 dB level for sound carriers at 32,90 MHz and 33,40 MHz
- Constant group delay

2.2.2.5.5. G1975 (IF Filter for Intercarrier Applications)

Standard

- B/G

Pin configuration
1 Input
2 Input - ground
3 Chip carrier - ground
4 Output
5 Output

Features

- TV IF filter with Nyquist slope and sound shelf
- Picture carrier at 38.90MHz

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- Reduced group delay predistortion as compared with standard B/G, half

2.2.2.6. SMPS

2.2.2.6.1. PRIMARY BLOCK

AC power applied via AC inlet, line filter components prevent chassis from incoming noise of AC line, also prevents AC line against created noises by TV. Bridge rectifier and bulk capacitor converts AC voltage to DC voltage. Applied DC voltage to primary winding is then swicthed via MOSFET by primary controller in a controlled manner.

SMPS controller works on quasi-resonant PWM and gets first supply voltage from AC line (SMPS Controller supply). Controller drives MOSFET according to feedback information supplied by shunt regulator and opto-coupler, according to that information adjusts on-time of MOSFET for required power. After the start-up in normal operation mode SMPS controller is supplied by SMT.

Primary block consist of following main parts,

AC Inlet (PL800),

Fuse (F800),

Varistor (R800),

Line Filter For EMC (C801,L800,C800),

SMPS Controller (IC801),

SMPS Controller supply for first Start-up (R807),

Bridge Rectifier (D811,D813,D814,D816),

Rectifier For SMPS Controller(D801),

Bulk Cap (C806),

Clamping Circuitry (R809,C812,C813,C817),

SMT (Switch Mode Transformer) (TR800),

SMT Driver MOSFET (Q800),

Current Sense Resistor (R812),

Protection Components for MOSFET Failure (D815,D812,R811)

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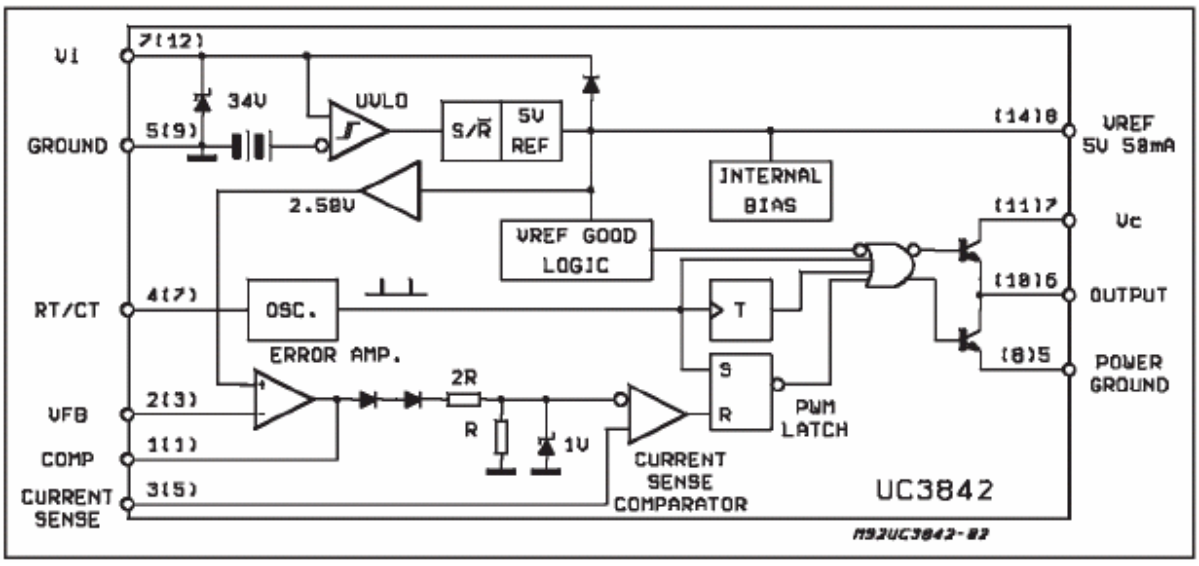
2.2.2.6.1.1. SMPS CONTROLLER (UC3842)

TheUC3842 of control IC providesthe necessary features to implement off-line or DC to DC fixed frequency current mode controlschemes witha minimal externalparts count. Internallyimplemented circuit sincludeundervoltagelockout featuring start-up current less than 1 mA, a precision reference trimmed for accuracy at the erroramp input, logic to insure latched operation, a PWMcomparatorwhichalso providescurrentlimit control,anda totem pole output stage designed to source or sink high peak current. The output stage, suitable for driving N-ChannelMOSFETs, is low in theoff-state. Differencesbetweenmembers of this family are the under-voltage lockout thresholds and maximum duty cycle ranges. The UC3842 has UVLO thresholds of 16V (on) and 10V (off), ideally suited off-line applications. The UC3842 can operate to duty cycles approaching 100%.

Features

- Optimized for off-line and dc to dc converters
- Low start-up current (< 1 ma)
- Automatic feed forward compensation
- Pulse-by-pulsecurrent limiting
- Enhanced load response characteristics
- Under-voltage lockout withhysteresis
- Double pulse suppression
- High current totempole output
- Internally trimmed bandgap reference
- 500Khz operation
- Low Ro erroramp

Block Diagram



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ABSOLUTE MAXIMUMRATINGS

Symbol	Parameter	Value	Unit
V_I	Supply Voltage (low impedance source)	30	V
V_I	Supply Voltage (Ii < 30mA)	Self Limiting	
I_O	Output Current	±1	A
E_O	Output Energy (capacitive load)	5	µJ
	Analog Inputs (pins 2, 3)	– 0.3 to 6.3	V
	Error Amplifier Output Sink Current	10	mA
P_{tot}	Power Dissipation at $T_{amb} \leq 50$ °C (minidip, DIP-14)	1	W
P_{tot}	Power Dissipation at Tamb ≤ 25 °C (SO14)	725	mW
T_{stg}	Storage Temperature Range	– 65 to 150	°C
T_L	Lead Temperature (soldering 10s)	300	°C

2.2.2.6.1.2. MOSFET

The MTP3N60E used for voltage range 170-270V, The MTP6N60E used for voltage range 90 – 270V.

2.2.2.6.1.2.1. MTP3N60E

N–Channel Enhancement–Mode Silicon Gate

This advanced high voltage TMOS E–FET is designed to with stand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain–to–source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

Avalanche Energy Capability Specified at Elevated Temperature
Low Stored Gate Charge for Efficient Switching
Internal Source–to–Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
Source–to–Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–Source Voltage	V_{DSS}	600	Vdc
Drain–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–Source Voltage — Continuous — Non–repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Pulsed	I_D I_D I_{DM}	3.0 2.4 14	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	75 0.6	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C

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2.2.2.6.1.2.2. MTP6N60E

N–Channel Enhancement–Mode Silicon Gate

This high voltage MOSFET uses an advanced termination scheme to provide enhanced voltage–blocking capability without degrading performance over time. In addition, this advanced TMOS E–FET is designed to withstand high energy in the avalanche and commutation modes. The new energy efficient design also offers a drain–to–source diode with a fast recovery time. Designed for high voltage, high speed switching applications in power supplies, converters and PWM motor controls, these devices are particularly well suited for bridge circuits where diode speed and commutating safe operating areas are critical and offer additional safety margin against unexpected voltage transients.

- Robust High Voltage Termination
- Avalanche Energy Specified
- Source–to–Drain Diode Recovery Time Comparable to a Discrete Fast Recovery Diode
- Diode is Characterized for Use in Bridge Circuits
- IDSS and VDS(on) Specified at Elevated Temperature

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain–to–Source Voltage	V_{DSS}	600	Vdc
Drain–to–Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	600	Vdc
Gate–to–Source Voltage — Continuous — Non–Repetitive ($t_p \le 10$ ms)	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Continuous @ 100°C — Single Pulse ($t_p \le 10$ µs)	I_D I_D I_{DM}	6.0 4.6 18	Adc Apk
Total Power Dissipation Derate above 25°C	P_D	125 1.0	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	–55 to 150	°C
Single Pulse Drain–to–Source Avalanche Energy — Starting T_J = 25°C (V_{DD} = 100 Vdc, V_{GS} = 10 Vdc, I_L = 9.0 Apk, L = 10 mH, R_G = 25 Ω)	E_{AS}	405	mJ
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.0 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T_L	260	°C

2.2.2.6.2. SECONDARY BLOCK

Switching primary winding of SMT induces voltages to secondary windings of SMT. Induced voltages are then rectified by secondary recitification diodes and capacitors.

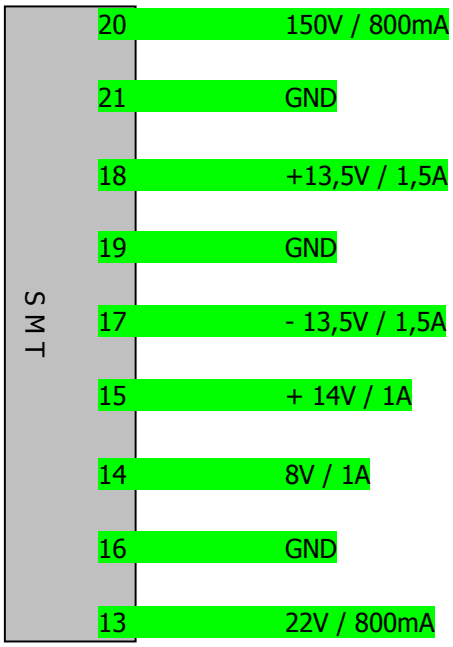
Secondary block consist of following main parts,

Optocoupler for sensing stand-by (IC805),(Optional) Only use for less than 3W models in Std_by (IC801,IC805,R825,R824,R826,R817,C836,C835,R822,Q804,Q805,Q806,R823,R820, R821,R819,D818,D817,D819 also are not available if there is no optocoupler)

Rectifier and DC line Components for B+ (C821,C822,C824,C832,D804,L804,R815),
Audio +12 Supply Rectifiers and DC line Components (C831,C826,C827,C828,C831,R814,D807)

+ 11 Supply Rectifiers and DC line Components (D806,C823,C825),

+ 6V Controller Supply Rectifiers and DC line Components at **Stand by Mode** (D805,C826,C830),



Power Supply Performance

USABLE MIN & MAX OPERTAING VOLTAGES (170 V- 270V)	170 V. min , 270 V. max
DROP OUT VOLTAGE	155 V.
START UP VOLTAGE	170 V.
POWER CONSUMPTION	< 1W in Stand-by, 160W max.
SMPS OUTPUT VOLTAGES	± 0,5 V. of design value
SMPS FET DRAIN VOLTAGE	% 90 of MOSFET spec.
SMPS FET GATE VOLTAGE	% 90 of MOSFET spec.
SMPS FET OPERATING FREQUENCY	Fix

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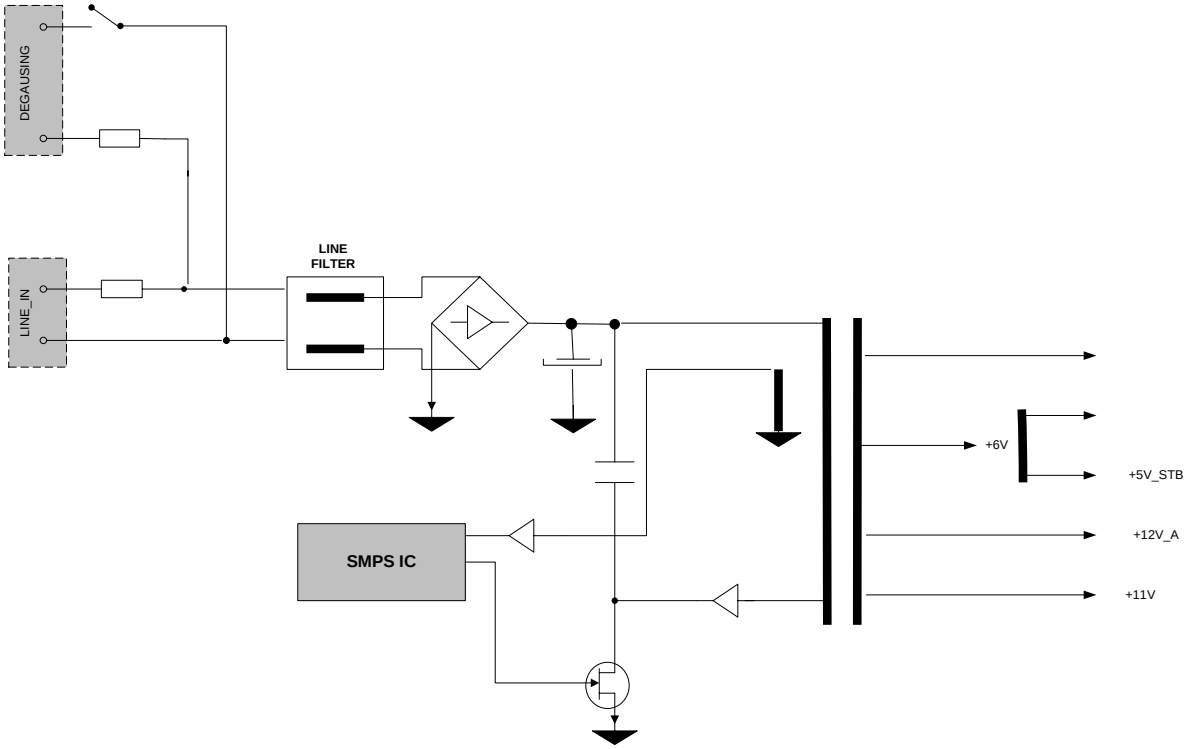
2.2.2.6.3. SMPS Block Diagram



2.2.2.7. DEFLECTION

2.2.2.7.1. HORIZANTAL DEFLECTION

Deflection block consist of following main parts,

Horizontal driver transistor (Q600),
Horizontal driver (L600),
HOT (Horizontal Output Transistor) (Q603),
FBT (TR600),
Linearity Coil (L601),
Flyback Capacitors (C611),
S-correction capacitor (C622),
Modulated S-correction capacitor (C623),
Hdrive signal is buffered and applied to line driver transistor by a capacitor.
Line driver produces necessary base currents, parallel diode to base series resistor speeds up the reverse base current.
UOCII has soft-start and soft-stop features to have more safe operation. There are two base current adjustment resistors on the circuit. Collector current differs according to CRT sizes .

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Tube dependent components are choosen to fit best picture performance by keeping;
11-12usec. Flyback time,
Max. 1300V. collector voltage (peak-detect mode measurement)

2.2.2.7.2. MD1803DFX

HIGH VOLTAGE NPN POWER TRANSISTOR FOR STANDARD DEFINITION CRT DISPLAY

Features

- State-Of-The-Art Technology: – Diffused collector "ENHANCED GENERATION"
- More stable performance versus operating temperature variation
- Low base drive requirement
- Tighter hFE range at operating collector current
- Fully insulated power package U.L. compliant
- Integrated free wheeling diode
- In compliance eith the 2002/93/EC EUROPEAN DIRECTIVE

Internal Schematic Diagram

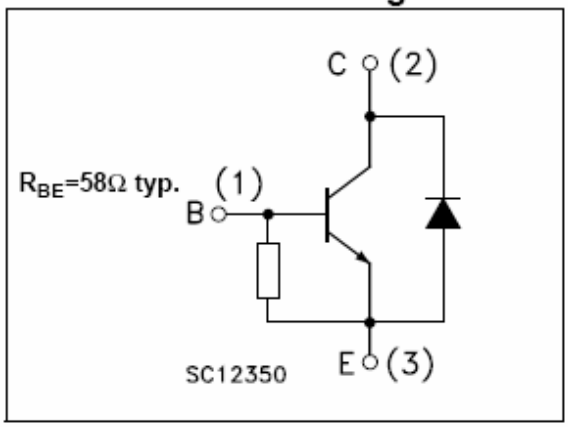

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Table 1. Absolute Maximum Rating

Symbol	Parameter	Value	Unit
V_{CES}	Collector-Emitter Voltage (V_{BE} = 0)	1500	V
V_{CEO}	Collector-Emitter Voltage (I_B = 0)	700	V
V_{EBO}	Collector-Base Voltage (I_C = 0)	7	V
I_C	Collector Current	10	A
I_{CM}	Collector Peak Current (t_P < 5ms)	15	A
I_B	Base Current	5	A
P_{TOT}	Total dissipation at T_c = 25°C	57	W
V_{isol}	Insulation Withstand Voltage (RMS) from all three Leads to External Heatsink	2500	V
T_{stg}	Storage Temperature	-65 to 150	°C
T_J	Max. Operating Junction Temperature	150	

Table 2. Thermal Data

Symbol	Parameter		Value	Unit
$R_{thj\text{-}case}$	Thermal Resistance Junction-Case	Max	2.2	°C/W

Table 3. Electrical Characteristics

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector Cut-off Current (V_{BE} = 0)	V_{CE} = 1500V V_{CE} = 1500V T_c= 125°C			0.2 2	mA mA
I_{EBO}	Emitter Cut-off Current (I_C = 0)	V_{EB} = 5V	75		100	mA
$V_{(BR)EBO}$	Collector-Emitter Breakdown Voltage (I_C = 0)	I_E = 700 mA	7			V
$V_{CE(sat)}$ *Note 1*	Collector-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A		3	5	V
$V_{BE(sat)}$ *Note 1*	Base-Emitter Saturation Voltage	I_C = 5 A I_B = 1.25 A			1.2	V
h_{FE}	DC Current Gain	I_C = 1 A V_{CE} = 5 V I_C = 5 A V_{CE} = 1 V I_C = 5 A V_{CE} = 5 V	5	18 5	8	
V_f	Diode Forward Voltage	I_F= 5 A		1.5	2	V
t_s t_f	INDUCTIVE LOAD Storage Time Fall Time	I_C = 4A f_h = 16KHz $I_{B(on)}$ = 0.6A $V_{BE(off)}$ = -2.5V $L_{BB(off)}$ = 4.5µH		2.5 0.35		µs µs

1 Pulsed duration = 300 µs, duty cycle ≤1.5%.

2.2.2.7.3. FBT

Operating Ampient Temperatue : -10°C.....+60°C
Stroge Ampient Temperature : -20°C.....+80°C
Operating Horizantal Frequency : 15.625KHz ±0.5KHz

INDUCTANCE (Between pin1 to pin3) : 3.02mH ± %8
INTERNAL RESISTANCE : Max. 2.2Ohm Regulation:Max.%10
FLYBACK TIME : 11.5µsec
COLLECTOR VOLTAGE : 1000Vp_p
FOCUS VOLTAGE RANGE % OF EHT: min.≤18.2 max.≥34.6
DEFLECTION CURRENT : 3.1Ap_p max.

AUXLIARY OUTPUTS:

Heater Voltage : 6.3Vrms / max 750mA
RGB Supply : +200V / max 30mA ±%5
Vertical Supply : +14V / max 1A ±%5
Vertical Supply : -14V / max 1A ±%5
Auxliary Voltage : +9V / max 1A ±%5
Tuning Voltage : +33V max 100mA ±%5

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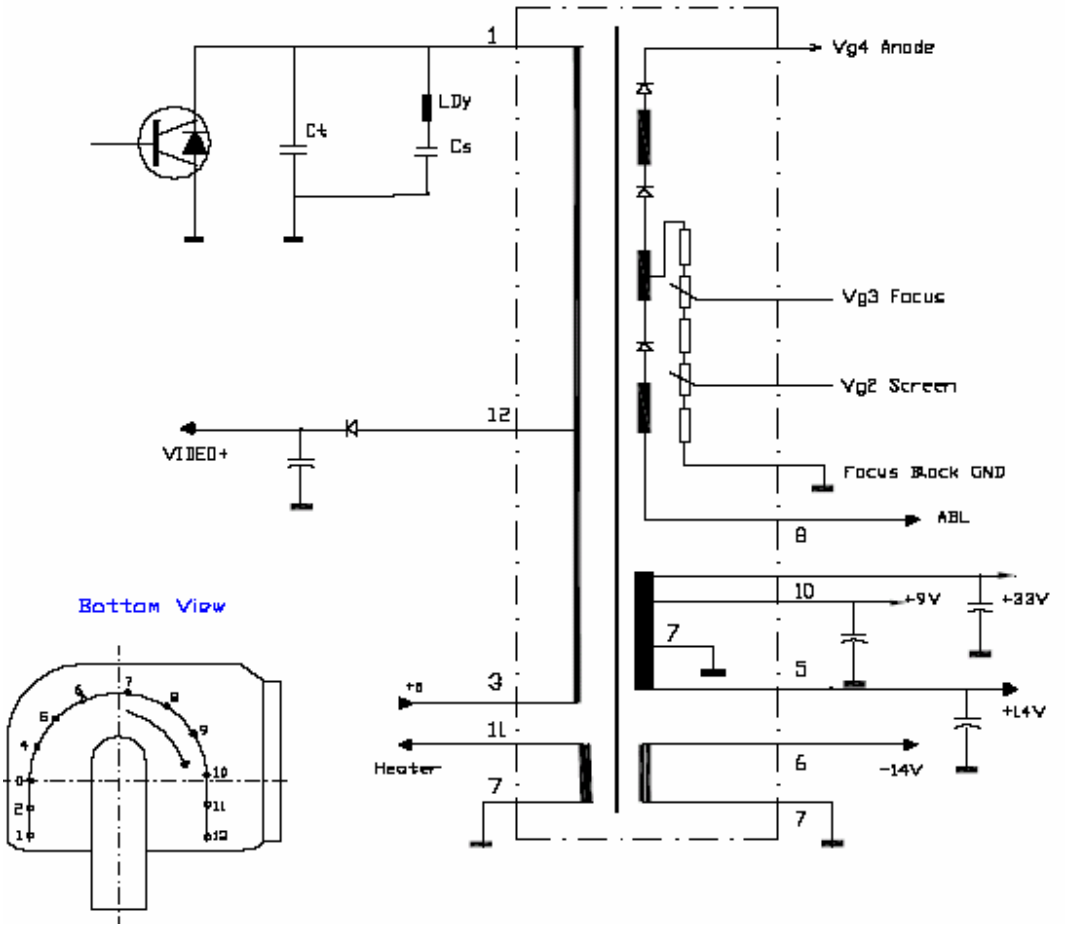
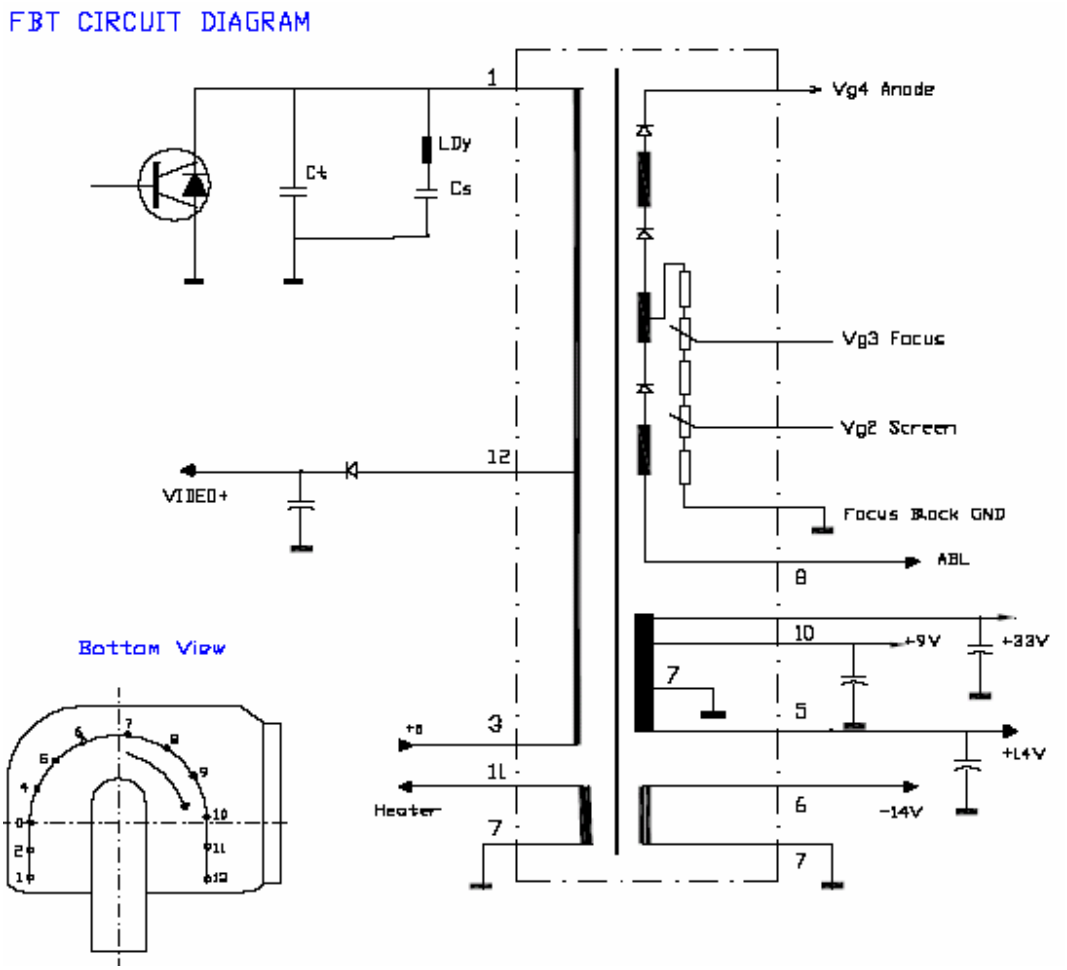
FBT CIRCUIT DIAGRAM





2.2.2.7.4. AN15524A (VERTICAL DEFLECTION OUTPUT)

The AN5524A (TV vertical deflection output circuit) is a monolithic integrated circuit designed for vertical deflection output, such as TV and display.

Features

- Built-in Pump-up circuit
- Built-in Thermal protection circuit
- Maximum deflection current = 1.6Ap-p
- Dimple forming type :
  Advantages : a) Withstand repeated movements between the body and the solder joint of the IC (when a heat-sink is used).
  b) Better vibration absorber (eg. CTV installed in the bus/coach).
- VCC operating range : 12V ~ 30V

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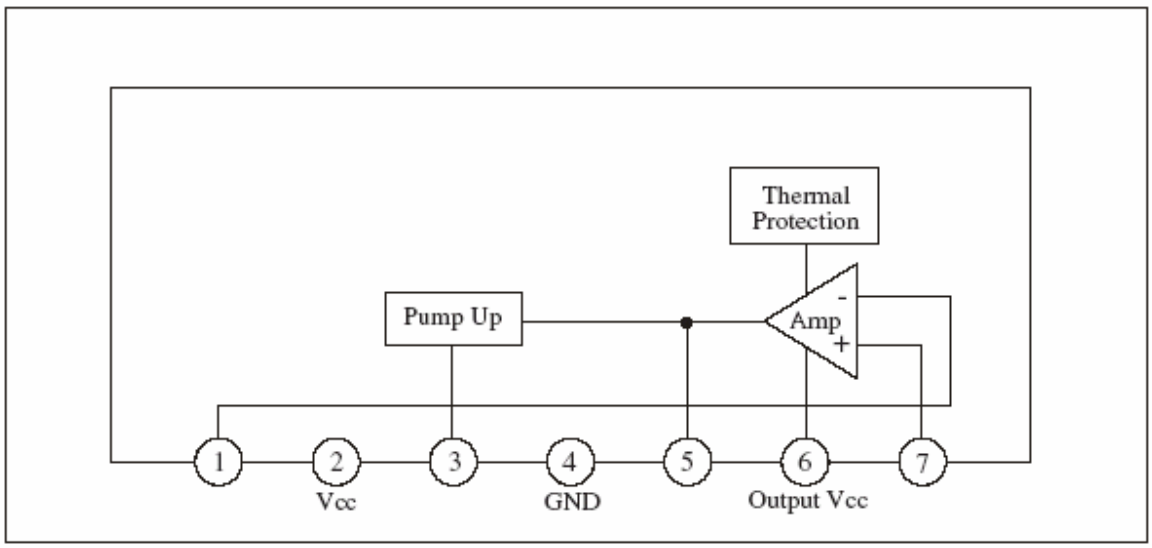
■ Block Diagram



■ Absolute Maximum Ratings (Ta=25°C)

Item	Symbol	Rating		Unit
Supply Voltage	V_{CC}	30		V
Supply Current	I_{CC}	360		mA
Power Dissipation (Ta=70°C in free air, without heat sink)	P_D	1.5		W
Operating Ambient Temperature	Topr	-20 ~ +70		°C
Storage Temperature	Tstg	-55 ~ +150		°C
Circuit Voltage	V_{5-4}	0	70	V
	V_{6-4}	0	70	
	V_{7-4}	0	V_{2-4}	
	V_{1-4}	0	V_{2-4}	
Circuit Current	I_5	-1.5	1.5	Ao-p
	I_3	-1.1	1.1	

■ Pin

Pin No.	Pin Name
1	Inverting Input
2	V_{CC}
3	Pump-up Output
4	GND
5	Vertical Output
6	Vertical Output Power Supply
7	Non-inverting Input

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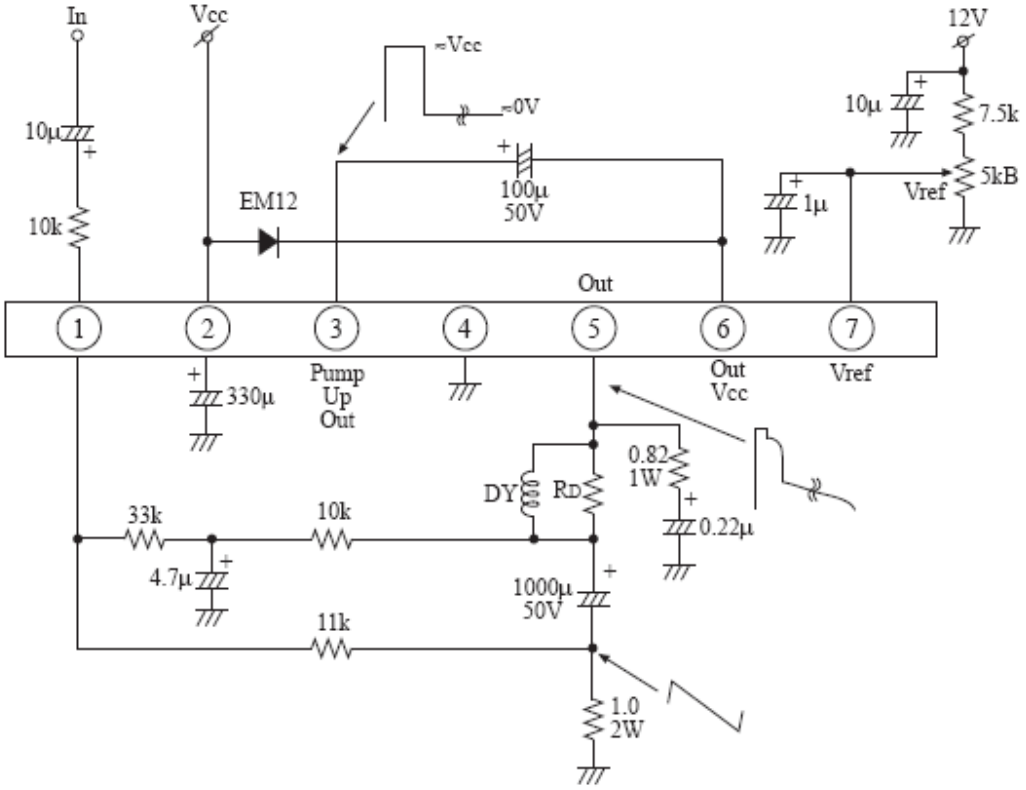


2.2.2.8. CRT BOARD

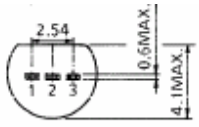
Transistors are used for amplifying RGB signals.

2SC2482 For High Voltage Switching And Amplifier Applications:

- High Voltage : $V_{(BR)}$=300V.
- Small Collector Output Capacitance : C_{ob}=3.0pF (typ.)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Collector-Base Voltage	V_{CBO}	300	V
Collector-Emitter Voltage	V_{CEO}	300	V
Emitter-Base Voltage	V_{EBO}	7	V
Collector Current	I_C	100	mA
Base Current	I_B	50	mA
Collector Power Dissipation	P_C	900	mW
Junction Temperature	T_j	150	°C
Storage Temperature Range	T_{stg}	−55~150	°C



1. EMITTER
2. COLLECTOR
3. BASE

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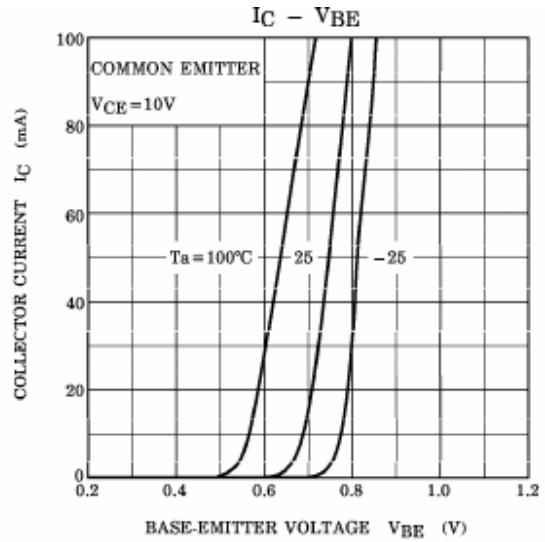
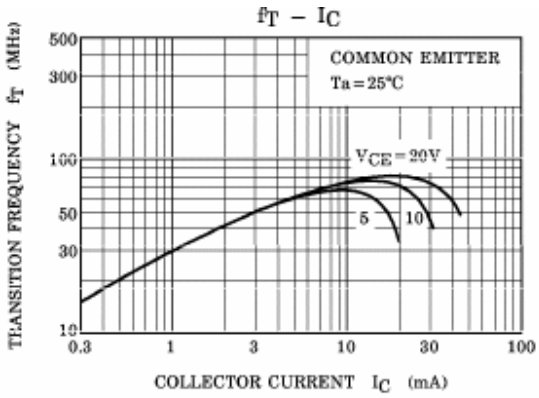
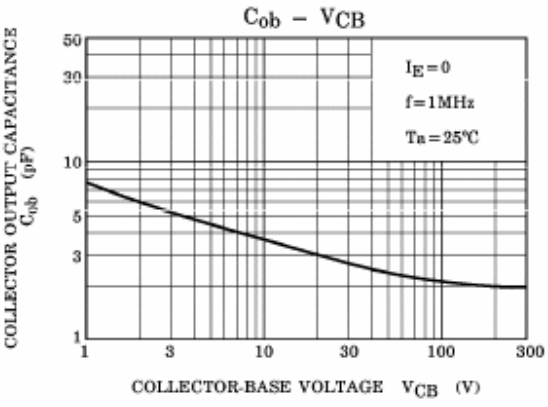
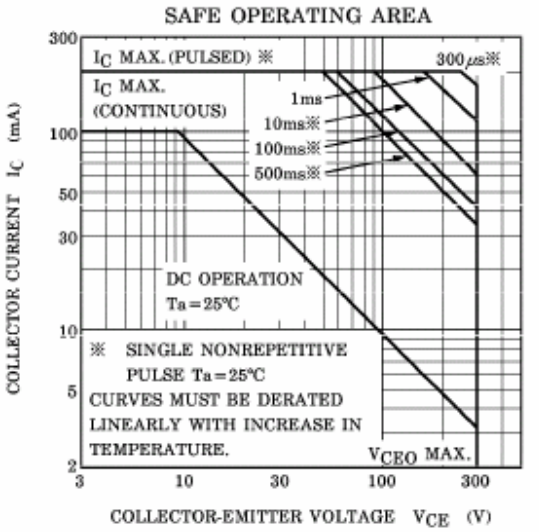
ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Collector Cut-off Current	I_{CBO}	V_{CB}=240V, I_E=0	—	—	1.0	μA
Emitter Cut-off Current	I_{EBO}	V_{EB}=7V, I_C=0	—	—	1.0	μA
DC Current Gain	$h_{FE\,(1)}$	V_{CE}=10V, I_C=4mA	20	—	—	
	$h_{FE\,(2)}$	V_{CE}=10V, I_C=20mA	30	—	150	
Collector-Emitter Saturation Voltage	$V_{CE\,(sat)}$	I_C=10mA, I_B=1mA	—	—	1.0	V
Base-Emitter Saturation Voltage	$V_{BE\,(sat)}$	I_C=10mA, I_B=1mA	—	—	1.0	V
Transition Frequency	f_T	V_{CE}=10V, I_C=20mA	50	—	—	MHz
Collector Output Capacitance	C_{ob}	V_{CB}=20V, I_E=0, f=1MHz	—	3.0	—	pF









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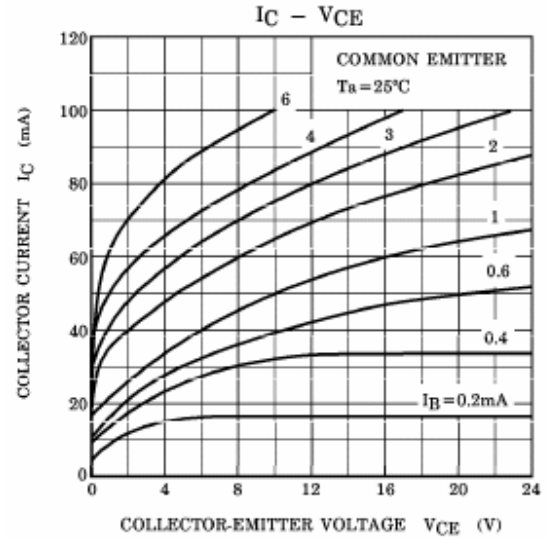

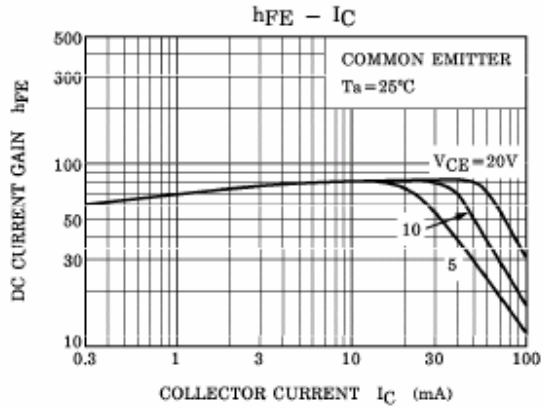

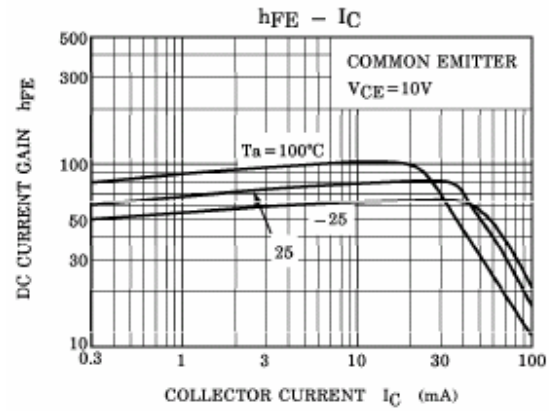

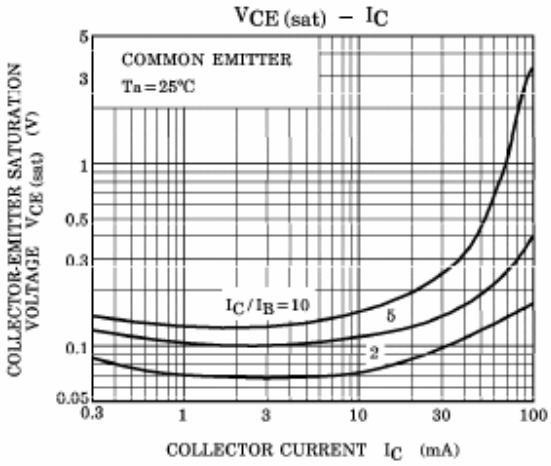

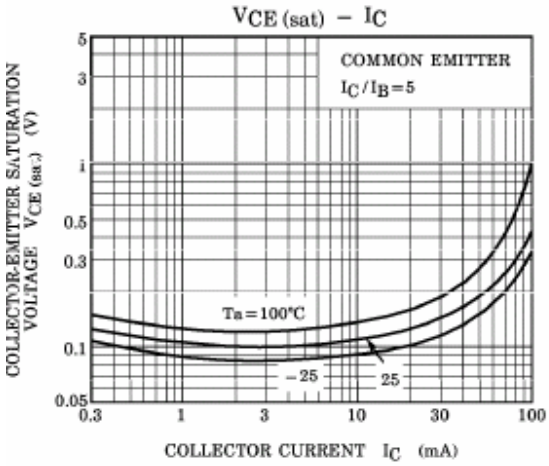

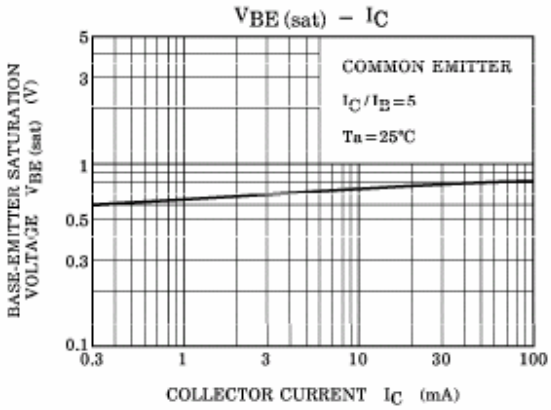

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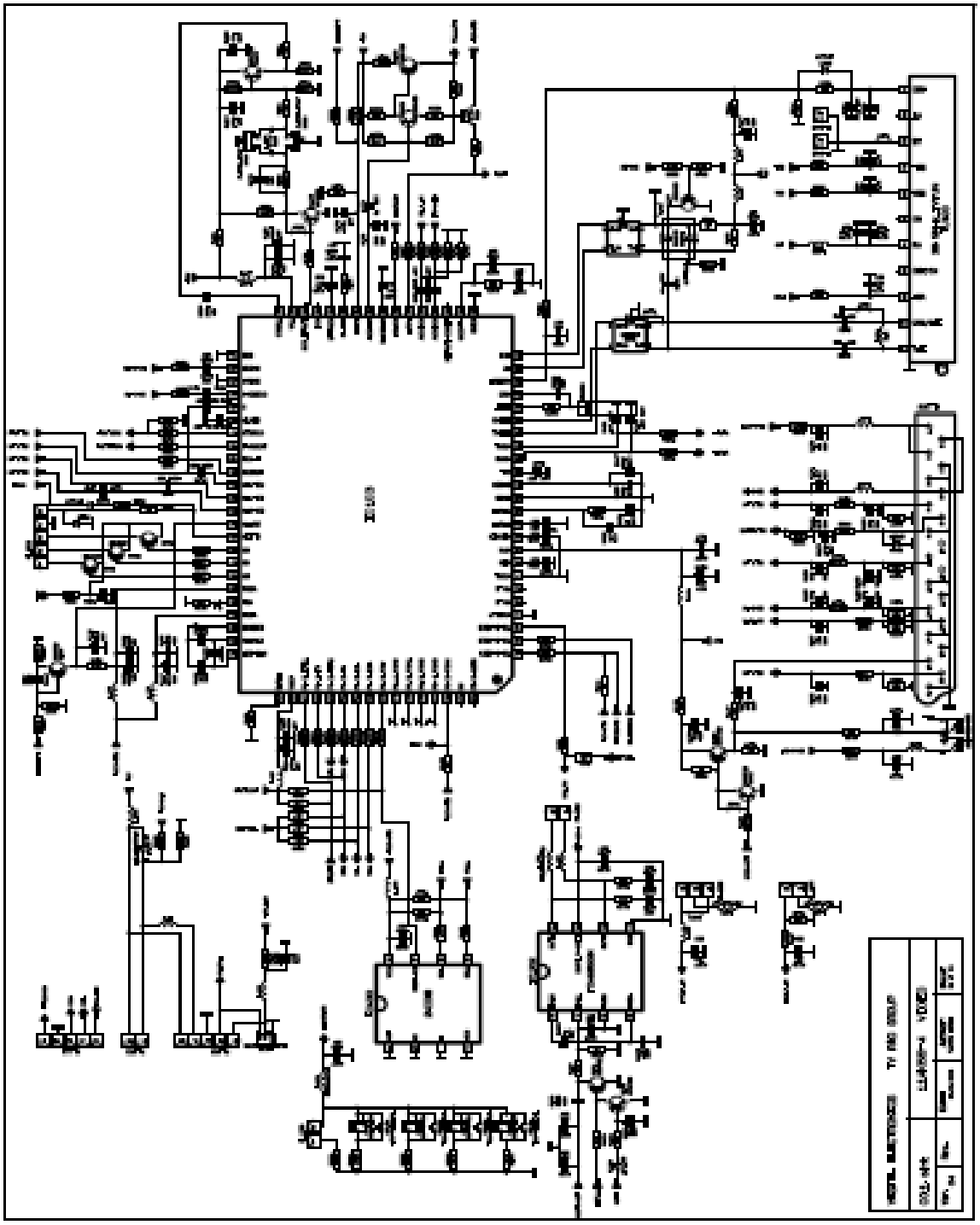
2.2.3. AK56 Chassis Scematics

2.2.3.1. Part1



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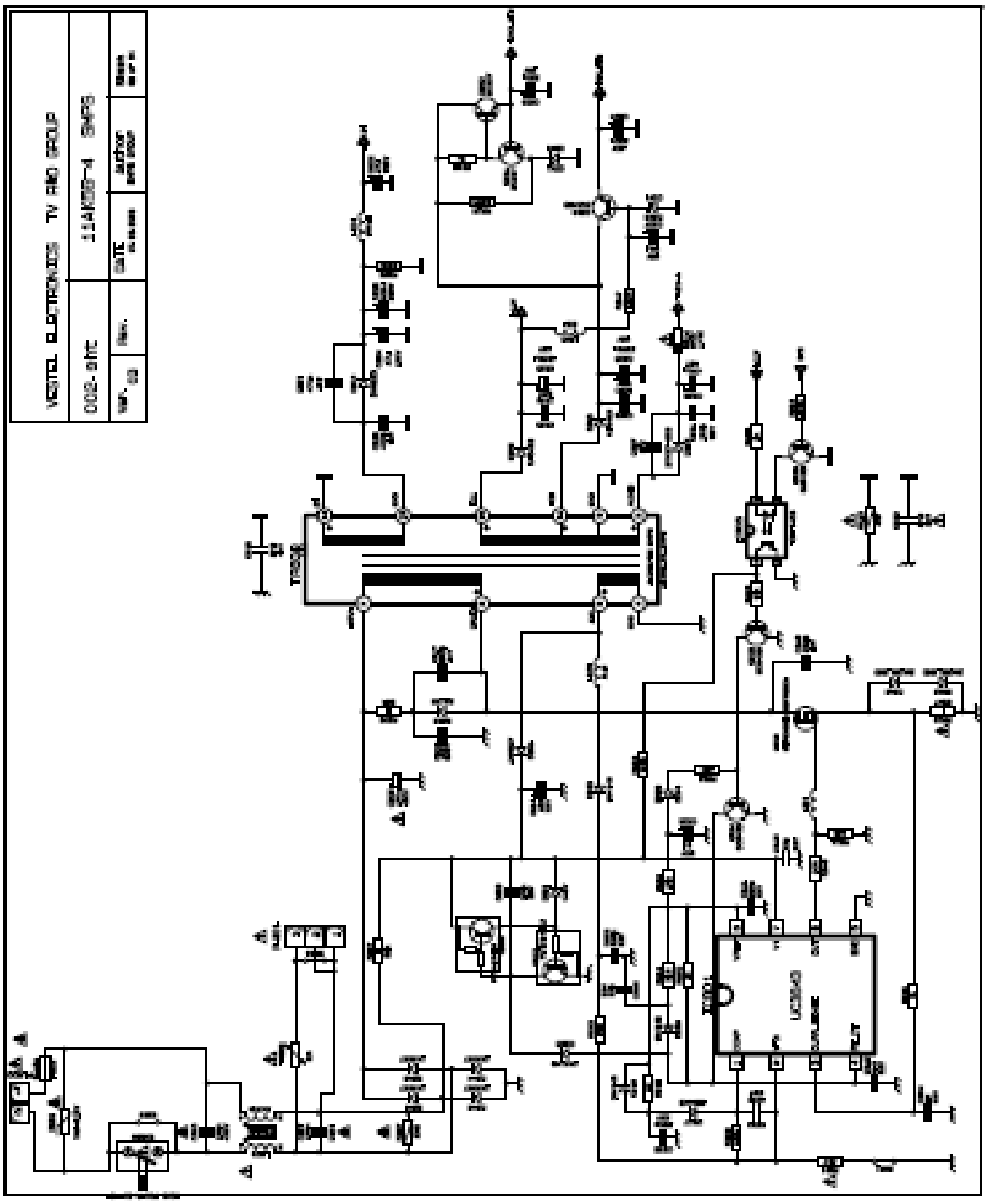

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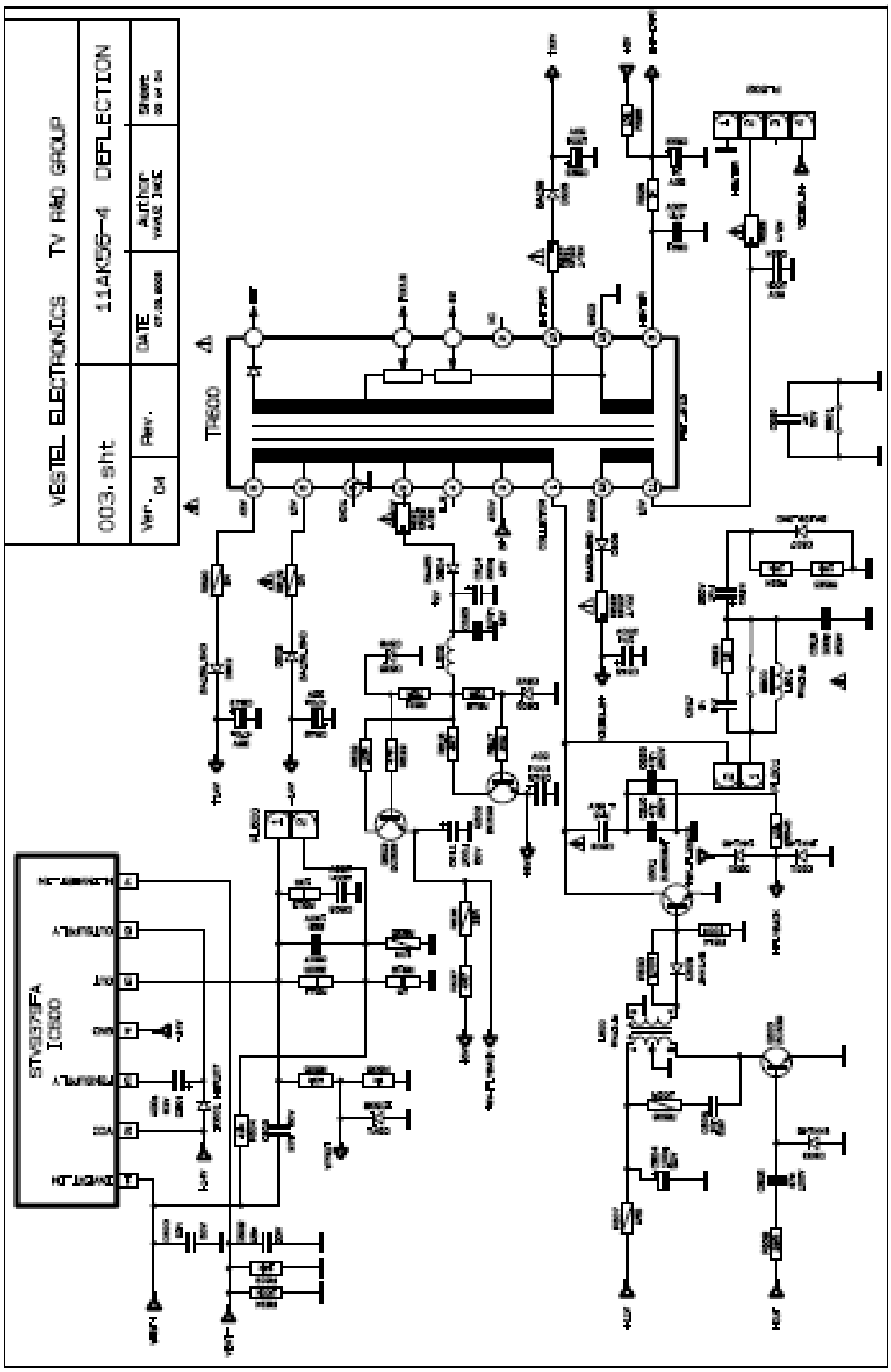

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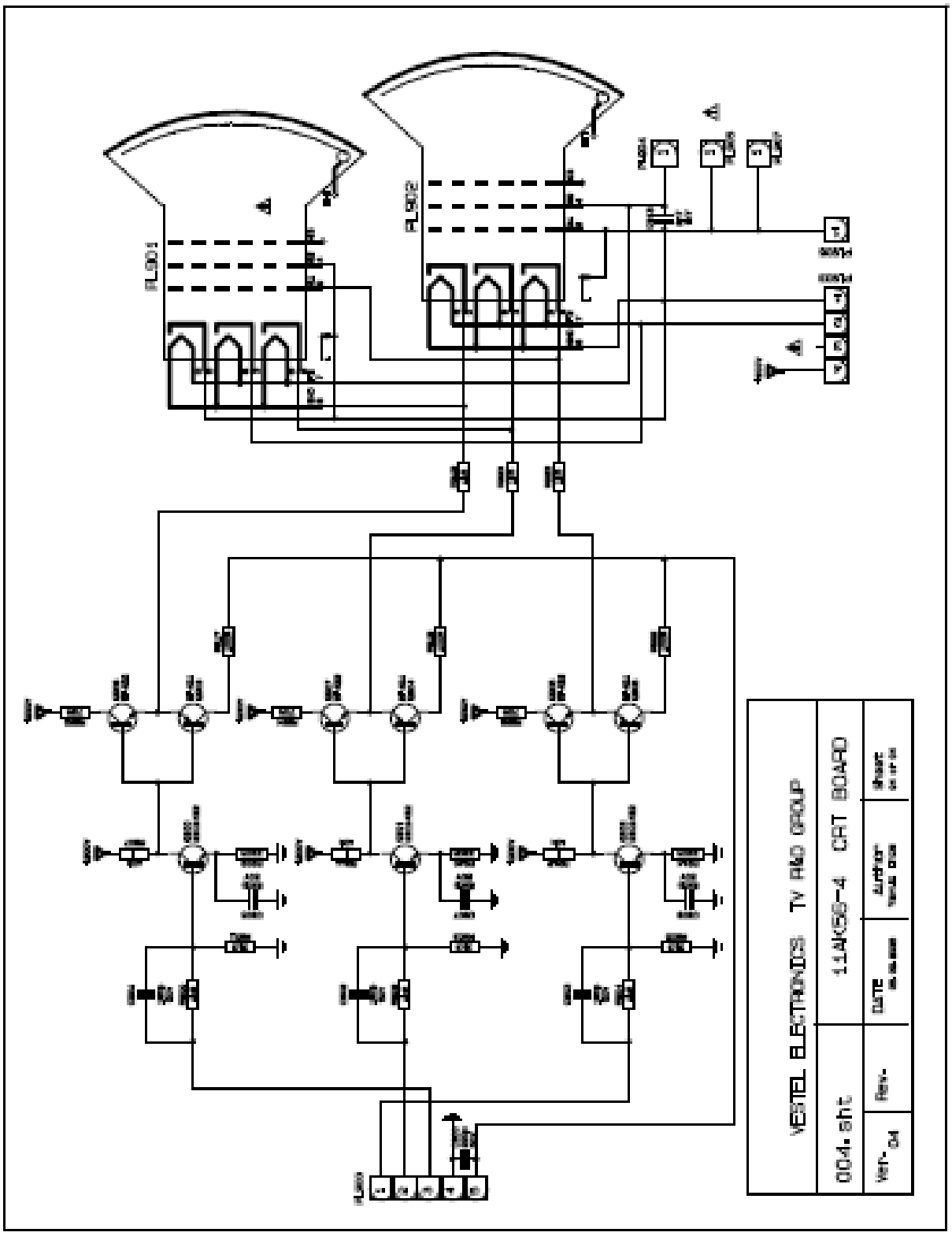
2.2.3.4. Part4



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2.3. Service Menu

To enter the Service Nenu, open main menu and press 4, 7, 2, 5 buttons from remotecontrol.

S-No	OSD	Definition	Possible Settings	Default
001	FAPS	First APS	ON = Active OFF = In-active	OFF
002	ISPM	I2C Mode	OFF	OFF
003	INIT	Resetting software and hardware	ON = Enable resetting OFF = Disable resetting	OFF

Table 1 Init

S-No	OSD	Definition	Possible Settings	Default
004	AGCSPD	IF AGC speed	0 = Slow 1 = Standard 2 = Fast 3 = Fastest	1
005	AGCTO	AGC Take over	0..63	31

Table 2 AGC Service settings

S-No	OSD	Definition	Possible Settings	Default
006	COFF	Cut-Off setting	0..63	32

Table 3 VG2 Alignment Service settings

S-No	OSD	Definition	Possible Settings	Default
007	VERT SLOP	Vertical slope (VSL), SBL bit should be keyed to half-blank.	0..63	32
008	SCORRECTION	S-correction	0..63	32
009	VERT SHIFT	4:3 vertical shifting for Wide Screen	0..63	32
010	VERT AMP	Vertical Amplitude	0..63	32
011	HOR SHIFT	Horizontal shifting	0..63	32

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S-No	OSD	Definition	Possible Settings	Default
012	VERT SHIFT16	16:9 vertical shifting for Wide Screen	0..63	32
013	VERT AMP16	16:9 Horizontal amplitude	0..63	32
014	RGB HSH	In RGB mode with 50 Hz, horizontal shifting	0..63	37
015	RGB HSH60	In RGB mode with 60 Hz, horizontal shifting	0..63	37
016	60HZ HSH 43	In 4:3 MODE with 60 Hz, horizontal shifting	0..63	31
017	60HZ VSH 43	In 4:3 MODE with 60 Hz, vertical shifting	0..63	31
018	60HZ VA 43	In 4:3 MODE with 60 Hz, vertical amplitude	0..63	31
019	60HZ VSH 169	In 16:9 MODE with 60 Hz, vertical shifting	0..63	31
020	60HZ VA 169	In 16:9 MODE with 60 Hz, vertical amplitude	0..63	31

Table 4 Geometry Service settings

S-No	OSD	Definition	Possible Settings	Default
021	QSS	Switching the mode of the QSS amplifier	ON = QSS Active OFF = QSS In-Active	ON
022	OIF	DC offset correction at IF-PLL	0..63	29
023	IF	PLL demodulator frequency	0 = 58.75 MHz 1 = 45.75 MHz 2 = 38.90 MHz 3 = 38.00 MHz 4 = 33.40 MHz 5 = 42.00 MHz 6 = 33.90 MHz 7 = 48.00 MHz 8 = EXTERNAL	2
024	OFR	Frequency Entry Activation: Frequency mode which is value Tuning Mode item on the Installation menu can be enabled or disabled by OFR.)	ON = Active OFF = In-Active	ON
025	FFI	Fast filter IF-PLL	ON = Fast time constant OFF = Normal time constant	OFF
026	BS1	Please look at the related Tuner specification for necessary adjustments.	0..15	1

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S-No	OSD	Definition	Possible Settings	Default
027	BS2	Please look at the related Tuner specification for necessary adjustments.	0..15	2
028	BS3	Please look at the related Tuner specification for necessary adjustments.	0..15	4
029	CB	Please look at the related Tuner specification for necessary adjustments.	0..255	142
030	B1-H	Please look at the related Tuner specification for necessary adjustments.	0..255	12
031	B1-L	Please look at the related Tuner specification for necessary adjustments.	0..255	32
032	B2-H	Please look at the related Tuner specification for necessary adjustments.	0..255	30
033	B2-L	Please look at the related Tuner specification for necessary adjustments.	0..255	2

Table 5 Tuning Service settings

S-No	OSD	Definition	Possible Settings	Default
034	FRAV	For AV, Peaking center frequency	0 = 2.7 Mhz 1 = 3.1 Mhz 2 = 3.5 Mhz	1
035	YSCM	For SECAM, Y-delay setting	0..15	12
036	YNTS	For NTSC, Y-delay setting	0..15	2
037	YPAL	For PAL, Y-delay setting	0..15	2
038	YAV1	For AV-1, Y-delay setting	0..15	4
039	YSVHS	For S-VHS-2, Y-delay setting	0..15	4

Table 6 Video Service settings

S-No	OSD	Definition	Possible Settings	Default
040	WPRC	For Cold, White point Red	0..63	32
041	WPGC	For Cold, White point Green	0..63	32
042	WPBC	For Cold, White point Blue	0..63	31
043	BLORB	Black level offset Red – Blue	0..63	32
044	BLOG	Black level offset Green	0..63	32
045	WPRN	For Normal, White point Red	0..63	37
046	WPGN	For Normal, White point Green	0..63	32
047	WPBN	For Normal, White point Blue	0..63	19
048	BLRB-RGB	For RGB, Black level offset Red – Blue	0..63	32
049	BLG-RGB	For RGB, Black level offset Green	0..63	32
050	WPRW	For Warm, White point Red	0..63	49

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S-No	OSD	Definition	Possible Settings	Default
051	WPGW	For Warm, White point Green	0..63	40
052	WPBW	For Warm, White point Blue	0..63	25
053	BLRB-YUV	For YUV, Black level offset Red – Blue	0..63	32
054	BLG-YUV	For YUV, Black level offset Green	0..63	32
055	WPRW-RGB	For RGB, White point Red	0..63	32
056	WPGW-RGB	For RGB, White point Green	0..63	40
057	WPBW-RGB	For RGB, White point Blue	0..63	32

Table 7 White tone adjustments

S-No	OSD	Definition	Possible Settings	Default
058	OSO	Switch-off at vertical overscan	ON = Enable Switch-off OFF = Disable Switch-off	ON
059	FSL	For vertical sync, Forced Slicing level	ON = Vertical slicing level fixed to 60% of sync amplitude OFF = Automatic vertical slicing level	OFF
060	PN8-STB	If option is ON TV can open from stanby when PIN8 is activated	OFF = feature is not avaliable ON = feature is avaliable	OFF
061	PWL	Peak white limiting	0..15	8
062	BPS	Bypass chroma base-band	ON = Bypass baseband chroma delay line OFF = Baseband chroma delay line active	OFF
063	CLPL	Soft clipping level	0 = 0% above PWL 1 = 5% above PWL 2 = 10% above PWL 3 = Off	0
064	CL	Cathode drive level	0..15	10
065	ST-LMI	Option for sleep timer last minute indicator	ON = last minute indicator appears on TV OFF = last minute indicator does not appear on TV	OFF

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S-No	OSD	Definition	Possible Settings	Default
066	DNMENU	Dynamic Menu Mode	ON = Dynamic Menu Enable OFF = Dynamic Menu Disable	OFF
067	OPC	Point black current system	ON = 1 point black current system OFF = 2 point black current system	OFF

Table 8 8 Bit Control Service settings

S-No	OSD	Definition	Possible Settings	Default
068	FAVI	FAV	ON = Active OFF = In-active	ON
069	BAVI	BAV	ON = Active OFF = In-active	OFF
070	BSVI	SVHS	ON = Active OFF = In-active	OFF
071	SSTDBG	BG sound standard	ON = Active OFF = In-active	ON
072	SSTDI	I sound standard	ON = Active OFF = In-active	ON
073	SSTDDK	DK sound standard	ON = Active OFF = In-active	ON
074	SSTDL	L- L prime sound standard	ON = Active OFF = In-active	ON

Table 9 Source Switching Service settings

S-No	OSD	Definition	Possible Settings	Default
075	TXHPOS	One page Teletext starting point setting	0..20	10
076	TXTBRI	Teletext brightness setting	0..63	32
077	TXTCON	Teletext contrast setting	0..15	0
078	LSEL1	Menu language setting	0..255	255
079	LSEL2	Menu language setting	0..255	255
080	-------			

Table 10 Teletext Service settings

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S-No	OSD	Definition	Possible Settings	Default
081	PWPRF	According to video and sound, when TV opening, fast startup and perfect startup	0..15 0 = Fast 15 = Perfect	10
082	PWRES	Opens from STANDBY.	ON = Opens depending on the last state OFF = Opens from STANDBY	ON

Table 11 Power Service settings

S-No	OSD	Definition	Possible Settings	Default
083	MAXCOL	Maximum color setting limiter at Picture menu	0..63	50
084	MAXBRI	Maximum brightness setting limiter at Picture menu	0..63	57
085	MINBRI	Minimum brightness setting limiter at Picture menu	0..63	20
086	MAXCON	Maximum contrast setting limiter at Picture menu	0..63	50

Table 12 Picture Service settings

S-No	OSD	Definition	Possible Settings	Default
087	SAVEFS	Saving Factory settings	OFF	OFF
088	LOADFS	Loading Factory setting	OFF	OFF
089	OAVL	OAVL = 0 (AVL is off and AVL line is not avaliable in sound menu) OAVL = 1 (AVL line is avaliable in sound menu) OAVL = 2 (AVL is on and AVL line is not avaliable in sound menu) Other values of OAVL work like OAVL =1	0-63	32
090	HTLSRC	Selection for hotel mode search HTLSRC = 0 (TV) HTLSRC = 1 (AV) HTLSRC = 2 (FAV) HTLSRC = 3 (SVHS) HTLSRC > 3 (HOTEL MODE NOT AVAILABLE)	0-63	32
091	HMAXVOL	Maximum volume for hotel mode	0-63	32
092	HDEFVOL	Volume level definition for hotel mode when tv is openning	0-63	32
093	RPO	Preover Shoot Ratio PSYS_RATIO_PRE_OVERSHOOT_MIN =0 PSYS_RATIO_PRE_OVERSHOOT_MAX =3	0-3	32

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094	PF	Peaking Frequency PF1-PF0 = 0 (2.7 Mhz) 1 (3.1 Mhz) 2 (3.5 Mhz) 3 (spare)	0-3	2
095	APSSND	Default value of sound standard in APS menu 0-> BG 1-> I 2-> DK 3-> L\L'	0-3	0

Table 13 Factory Service settings

2.3.1. TUNER Settings

	AK56 SERVICE MENU ITEMS							
	B1-H	B1-L	B2-H	B2-L	BS1	BS2	BS3	CB
Philips UV1316S MK3	12	50	30	2	1	2	4	142
LG TAEW-G002D	11	82	29	2	1	2	8	142
Thomson CTT5020	9	146	27	130	3	6	133	142
Samsung TECC2949PG28B	13	18	31	130	1	2	4	142
Samsung TECC2949PG35B	13	18	30	130	1	2	8	142
Alps TEDE9X226A	11	82	29	2	1	2	8	142
Alps TEDE9-004A	11	194	28	242	1	2	8	142
Samsung TECC2949PG40B	11	82	29	2	1	2	8	142
Samsung TECC2949PS40B	11	82	29	2	1	2	8	142

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Explanations	
B1H	High byte of VHF1-VHF3 cross-over frequency
B1L	Low byte of VHF1-VHF3 cross-over frequency
B2H	High byte of VHF3-UHF cross-over frequency
B2L	Low byte of VHF3-UHF cross-over frequency
BS1	Band switching byte for VHF1
BS2	Band switching byte for VHF3
BS3	Band switching byte for UHF
CB	Control byte

2.3.2. Adjustments

Geometry Adjustment: After adjusting 50Hz geometry items (between 007-011). NTSC 60 Hz geometry items (between 016-018) should be adjusted to determine NTSC 60Hz offset. NTSC offset is automatically calculated and stored in NVM. Later on, if we need to change 50Hz geometry settings, NTSC 60Hz geometry settings is automatically calculated by using NTSC offset. 16:9 mode geometry adjustment works like NTSC 60Hz geometry adjustment.

If press to menu button between 007-011 or 016-018 items. New geometry setting is stored and, 16:9 mode, RGB shift and NTSC geometry automatically calculated. RGB shift offset value is stored in software. Only NTSC offset and 16:9 mode offset values are stored in EEPROM.

AGC adjustment: Connect to tuner 60db broadcast and, press to blue button on AGCTO item. AGC is automatically adjusted.

Screen Adjustment: When yellow button is pressed in service menu. Vertical scan is disabled and related registers are updated. Thin line will be appeared on the screen. Then the screen potentiometer is gently adjusted until the thin line will be lightly disappeared When press to yellow button again, old register values are reloaded and vertical scan is enabled.

FOCUS Adjustment: TV is tuned to the signal. Then focus potantiometer (the upper pot on the rear side of the FBT transformer) is adjusted for optimum focusing drive.

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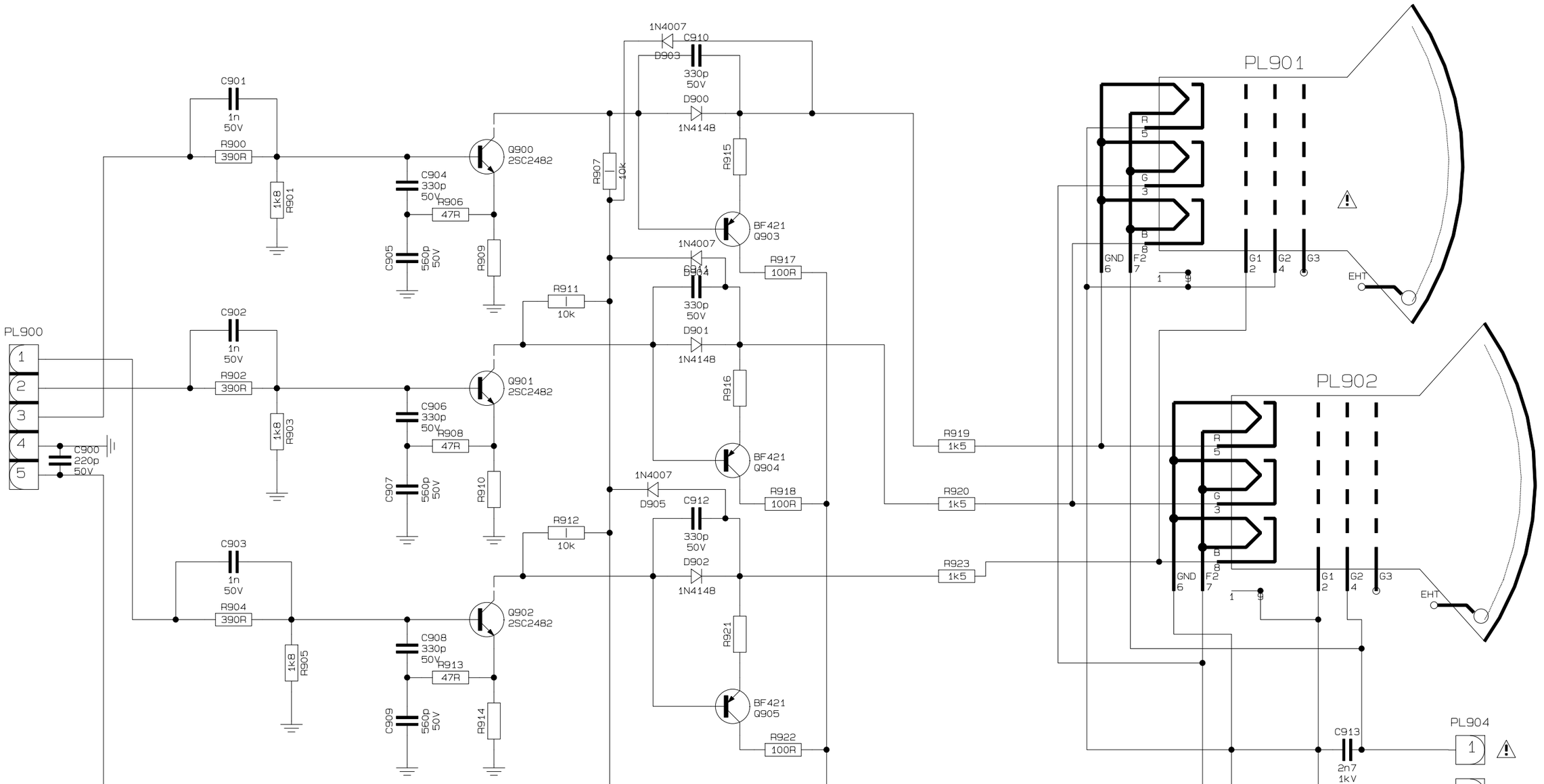

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004.sht		11AK56 CRT BOARD		
Ver. 01	Rev.	DATE 12.09.2005	Author Yavuz Ince	Sheet 04 of 04

VESTEL ELECTRONICS TV R&D GROUP				
003.sht		11AK56 DEFLECTION		
Ver. 01	Rev.	DATE 12.09.2005	Author Yavuz Ince	Sheet 03 of 04

STV9379FA
IC600
INVERT_IN
VCC
FBKSUPPLY
GND
OUT
OUTSUPPLY
N_INVERT_IN
VERT-
VERT+
R600 27k
R601 27k
R602 27k
R603 18k
C600 15n 50V
C602 15n 50V
C601 63V 100u
IC601 HER107
+14V
-14V
R604 12k
C603 27p 50V
PL600
R605 10k
VPROT
BZT55C5V1
IC602
R606 1k
R611 390R
C607 22n 100V
C608 100n 100V
R613 10R
R612 1R
+14V
BA159
D603
R620 0R22 1/2W
C613 35V 470u
TR600
45V
EHT
R619 0R47 1/2W
D602 BA159
C612 470u 35V
15V
-14V
+5V
IC604 78L05_TO92
GND1
C611 100u 50V
R616 4R7
+9V
BA159 D604
R621 0R22 1/2W
100V
FOCUS
Q602 BC639
R617 560R
R618 390R
C614 220u 16V
E_W
G2
+8V
C615 100u 50V
D605 8V2_ZENER
150V
NC
B+
COLLECTOR
EHTINFO
R627 0R22 1/2W
BA159 D608
C623 100u 50V
+33V
VIDEO_B+
R622 0R47 1/4W
BA159_SMD D606
C616 10u 250V
GND2
GND3
+11V
R607 1R5
C604 100u 50V
R608 100R
@Value L600
C606 10n 63V
R614 100R
Q601 BU2508AF
C609 7n5 1.6kV
C610 47n 250V
+5V
D600 1N4148
D601 1N4148
10k R615
HFLYBACK
PL601
10V
HEATER
R626 1k
9k1 R628
+8V
EHT_INFO
C621 47n 50V
C622 47n 50V
FBT_AK19
C617 1n 1kV
R623 1k
250V 10u
C619
S600
L601
@Value
C618 330n 250V
R624 15k
R625 15k
D607 BA159_SMD
C620 1n 50V
S601
R629 1/2W
C624 50V 100n
HEATER
VIDEO_B+
PL602
HOUT
R609 22R
C605 47n 100V
IC603 1N4148
R610 470R
Q600 BC639

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002.sht		11AK56 SMPS		
Ver. 01	Rev.	DATE 12.09.2005	Author SMPS GROUP	Sheet 02 of 04

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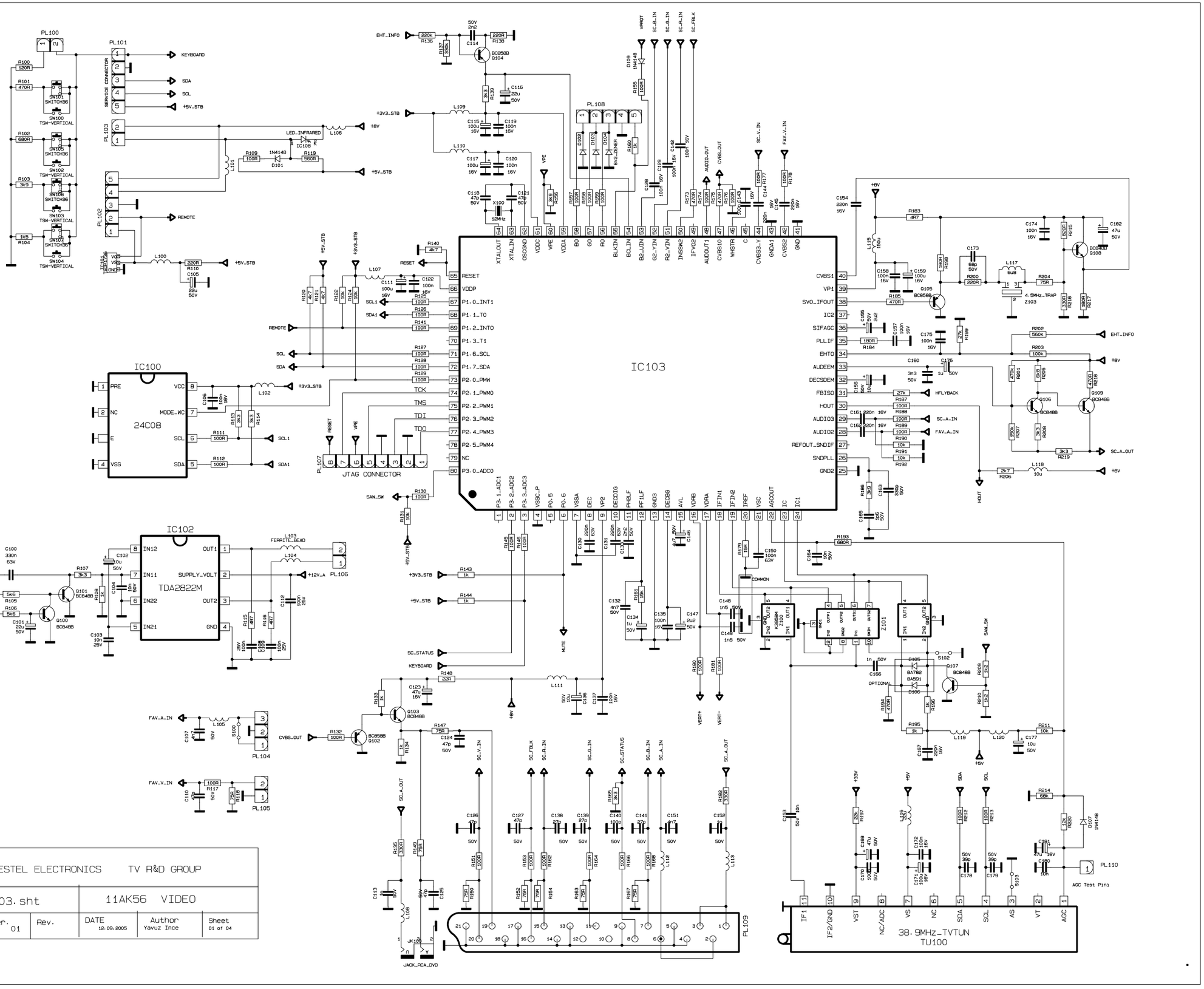
3.15A
F800
R800
VAR-510V
MONO_POWER_SWITCH
SW800
S800
C800
100n
400V
L800
Value
2x27m
TH800
9R
PL801
S803
400V
100n
C801
TR800
SMPS_AK56
C816
2n2
4kV
C821
470p
1kV
D804
BYM26D
C822
470p
1kV
C824
47u
160V
R815
33k
L804
22u
C832
33u
160V
B+
D811
1N4007
D813
1N4007
D816
1N4007
D814
1N4007
C806
100u
400V
R807
330k
R809
56k
C812
470p
630V
D802
BA159
C817
220p
1kV
1N4937
D801
L802
6u8
C814
10u
50V
D803
1N4148
L803
2u2
R803
22k
C809
220n
63V
C808
50V
22n
1N4148
D819
1M
R819
C835
220n
16V
1N4148
D817
1N4148
D800
R804
3k3
R805
1K
R820
10k
D818
BZT55C2V4
C836
1u
50V
R821
10k
R823
100k
IC801
R802
120k
C803
100p
50V
COMP
VFB
CURR_SENSE
RT_CT
VREF
V1
OUT
GND
UC3843
C811
220n
25V
C815
22n
50V
Q804
BC848B
Q805
BC848B
R822
10k
IC805
TCET110G
R825
1K
+11V
Q806
BC848B
R824
100k
+5V_STB
Q800
MTP6N50E/SSP7N50A
C819
330p
1kV
L801
10R
R810
R811
10k
R801
4K7
S801
C810
2n2
63V
R806
1K
C804
1n
50V
D815
BA159_SMD
D812
BA159_SMD
R812
0R33
R813
4M7
C820
2n2
4kV
D806
UF5402
C823
100n
50V
C825
1000u
16V
+11V
D805
UF5402
C826
100n
50V
C830
1000u
16V
R818
R20R
R816
1k
Q803
BC337
Q801
BC337
+3V3_STB
C833
220u
16V
BZT55C2V7
D810
C829
330p
1kV
BYV27-200
D807
C827
1n
1kV
50V
100n
C831
C828
470u
16V
R814
0R47
1/4W
+12V_A
Q802
BC548B
+5V_STB
16V
220u
C834
R817
330k
D809
BZT55C5V6


IC103
IC100
24C08
IC102
TDA2822M
PL100
PL101
PL102
PL103
PL104
PL105
PL106
PL107
PL108
PL109
JTAG CONNECTOR
JACK_RCA_DVD
IC108
SW100 TSW-VERTICAL
SW101 SWITCH36
SW102 TSW-VERTICAL
SW103 SWITCH36
SW104 TSW-VERTICAL
SW105 SWITCH36
KEYBOARD
SERVICE CONNECTOR
SDA
SCL
+5V_STB
REMOTE
LED_INFRARED
+6V
+3V3_STB
+12V_A
MUTE
SC_STATUS
KEYBOARD
CVBS_OUT
FAV_A_IN
FAV_V_IN
AUDIO_OUT
EHT_INFO
SC_A_IN
SC_A_OUT
SC_B_IN
SC_G_IN
SC_R_IN
SC_FBLK
SC_V_IN
SC_STATUS
AUDIO_OUT
CVBS_OUT
FAV_V_IN
VERT+
VERT-
HFLYBACK
SAW_SW
AGC Test Pin1
38.9MHz_TVTUN
TU100
4.5MHz_TRAP
Z103
K3958M
Z100
OPTIONAL
COMMON
VESTEL ELECTRONICS TV R&D GROUP
003.sht 11AK56 VIDEO
Ver. 01 Rev. DATE 12.09.2005 Author Yavuz Ince Sheet 01 of 04