AE-6B (KV-32LS65AUS) CHASSIS
OPERATION MANUAL

TRINITRON® COLOR TV
SONY®

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Chapter 1 AE-6B Chassis Concept

1.1 Features

This is a new Chassis but some circuits are referred from other chassis. The Deflection Circuit and the Back End (CXA2100) are based on AE-5 chassis. Besides, its Power Supply Circuit is almost the same as FE-2 chassis.

It is a 100 Hz FD Trinitron and Digital Plus (ABAB) model with 16:9 lifestyle cosmetic design concept. Its Digital Noise Reduction (DNR) allows users to reduce the picture noise visible in the broadcast signal.

Virtual Dolby sound effect can simulate the sound effect of "**Dolby Surround Pro logic**". **Dolby Surround** sound effect could be created by simulating the sound of four speakers with two speakers provided the broadcast audio signal is **Dolby Surround** encoded.

BBE High Definition Sound system enhances clarity, detail and presence of sound for better intelligibility and musical realism.

AE-6B chassis has Menu that is similar to FE-2 chassis. There is 1 Tuner for PIP.

Besides, it has Auto Format option that enables the aspect ratio of the screen to be automatically changed.

There are three Scarts (Scart 1, Scart 2 and Scart 3) at the rear, which are the 21-pin Euro connector. The pin diagram is shown as Figure 1.1. Scart 1 and Scart 2 are inputs for YUV while Scart 3 is input for S Video.

Figure 1.2 shows the board overview of AE-6B for KV-32LS65AUS model.

1.2 Specifications

Picture	Audio	Terminals	
100 Hz Digital Plus	**Right and left speaker**	**REAR**	
Digital Noise Reduction (DNR)	2X20W (Music Power)	1: 21-pin Euro Connector	Inputs for audio and video signals.
	2X10W (RMS)	(CENELEC Standard)	Inputs for YUV
			Outputs of TV video and audio signals.
Other Features	**Others**	2: 21-pin Euro Connector	Inputs for audio and video signals.
Teletext	Auto Volume Adjust		Inputs for YUV
Fastext/ TOPtext	Virtual Dolby		Outputs of TV video and audio signals (Monitor Out).
Sleep Timer	BBE	3: 21-pin Euro Connector	Inputs for audio and video signals.
PIP (1 Tuner)			Inputs for S Video.
Auto Format	**Remote Commander**		Outputs of TV video and audio signals (selectable).
	RM-934	Phono Jacks	Output connectors variable for audio signals.
		SIDE	
	Power Requirement	S Video Input	4 Pin DIN
	220 – 240V	Video Inputs	Phono Jacks
		Audio Inputs	Phono Jacks
		Headphone Jack	Stereo Mini Jack

1.3 21 Pin Connector

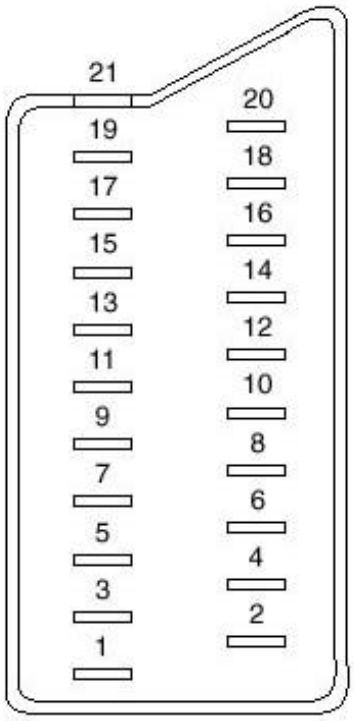


Figure 1.1 21-pin Euro connector

Pin No	Scart 1	Scart 2	Scart 3	Signal	Signal level
1	O	O	O	Audio output B (right)	Standard level: 0.5 V rms Output impedance: Less than 1kΩ*
2	O	O	O	Audio input B (right)	Standard level: 0.5 V rms Output impedance: More than 10kΩ*
3	O	O	O	Audio output A (left)	Standard level: 0.5 V rms Output impedance: Less than 1kΩ*
4	O	O	O	Ground (audio)	
5	O	O	O	Ground (blue)	
6	O	O	O	Audio input A (left)	Standard level: 0.5 V rms Output impedance: Less than 10kΩ*
7	O	●	●	Blue input	0.7 +/-3dB, 75Ω positive
8	O	O	O	Function select (AV control)	High state (9.5-12V): Part mode Low state (0-2V): TV mode Input impedance: More than 10kΩ Input capacitance: less than 2nF
9	O	O	O	Ground (green)	
10	O	O	O	Open	
11	O	●	●	Green	Green signal: 0.7 +/-3dB, 75Ω, positive
12	O	O	O	Open	
13	O	O	O	Ground (red)	
14	O	O	O	Ground (blanking)	
15	O	-	-	Red input	0.7 +/-3dB, 75Ω, positive
	-	O	O	(S signal Chroma input)	0.3 +/-3dB, 75Ω, positive
16	O	●	●	Blanking input (Ys signal)	High state (1-3V) Low state (0-0.4V) Input impedance: 75Ω
17	O	O	O	Ground (video output)	
18	O	O	O	Ground (video input)	
19	O	O	O	Video output	1V +/-3dB, 75Ω, positive sync 0.3V (-3+10dB)
20	O	-	-	Video input	1V +/-3dB, 75Ω, positive sync 0.3V (-3+10dB)
	-	O	O	Video input Y (S signal)	1V +/-3dB, 75Ω, positive sync 0.3V (-3+10dB)
21	O	O	O	Common ground (plug, shield)	

O Connected
● Not Connected (open)

* at 20Hz – 20kHz

1.4 Board Overview

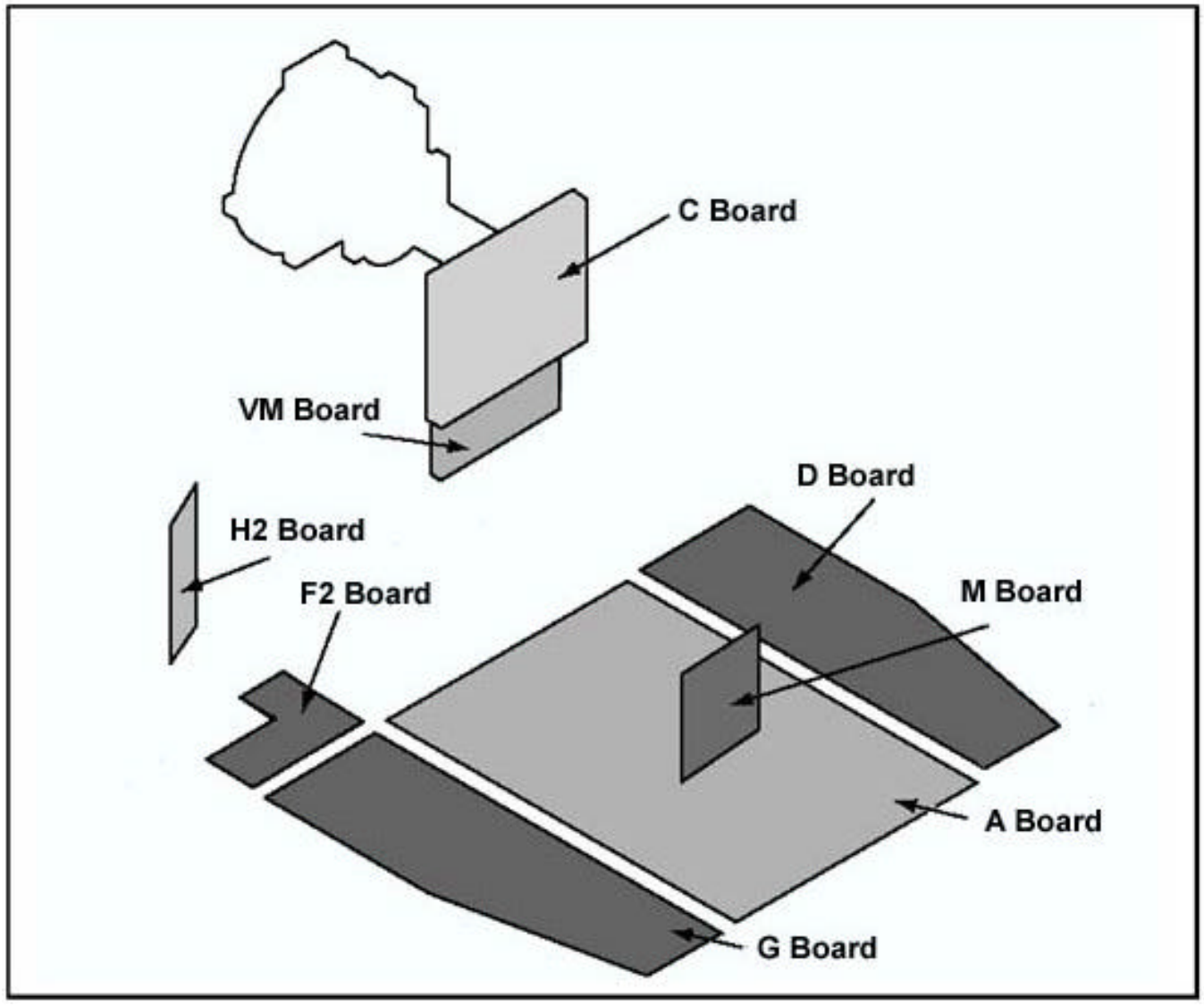


Figure 1.2 Board Overview (KV-32LS65AUS)

Chapter 2 Power Supply Circuit

2.1 Power Supply Block Overview

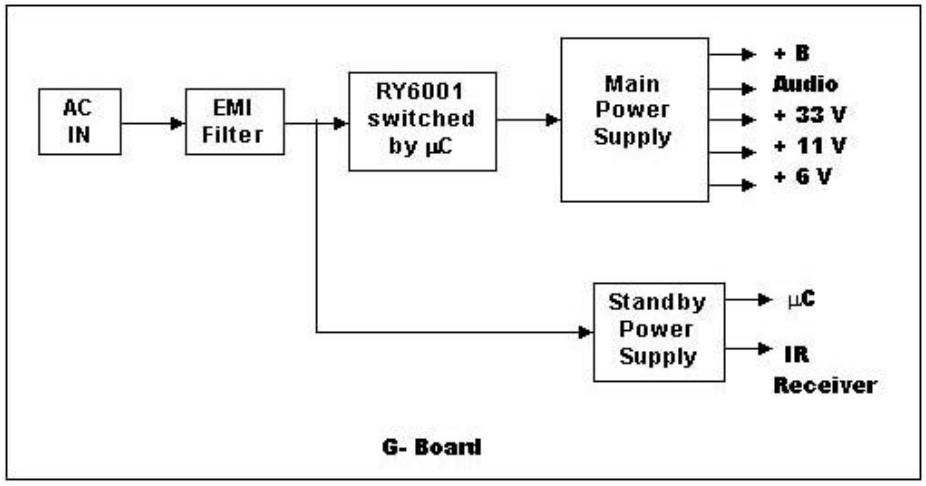


Figure 2.1 Power Supply Block Overview

2.2 Function Overview

The main power supply diagrams in AE-6B chassis are shown as Figure 2.2 and Figure 2.3. It is similar to FE-2 and LE-3 chassis. Meanwhile, the power supply circuit for AE-6B and AE-6D chassis is almost similar. The difference is there is an additional G1 board in AE-6D chassis.

The primary power supply on the AE-6B chassis G board consists of three parts:

1. Oscillator 2. Output stage 3. Regulator Stage

The oscillator starts up to produce an initial signal for the output stage. The output stage develops voltage to continue running the oscillator stage, supply the regulating stage and provide normal output for the TV. One of the normal TV outputs is used to start the secondary power supply.

Oscillator Start Up

The oscillator within IC6001 starts if the VSENSE input voltage at pin 1 is above 1.3 V_{DC} but less than 8 V_{DC}. The block diagram of IC6001 is shown in Figure 2.4.

Sample voltage from pin 18 is then used to run the internal oscillator. The initial frequency is approximately 230 kHz. The low amplitude initial oscillator signal is output IC6001 / pins 12 and 16 into the driver/output stage.

Driver / Output Stage

The oscillator voltage output at pins 12 and 16 use drivers Q6006 and Q6007 to develop T6002 secondary voltages. IC6001's oscillator will shut down if the driver transistor's current is excessive. To prevent premature shutdown, the timer capacitor C6007 (refer to Figure2.3) delays the shutdown.

VC1 Powers IC6001

Although the oscillator is running at the initial frequency of 200 kHz, there is insufficient current from T6002 to produce any unregulated output voltage because of the load. There is a little load on D6008 (refer to Figure 2.3). This voltage is returned to IC6001 / pin 8 (VC1) to serve as regulated +B for the IC.

IC6001 Normal Operation

At start up, IC6001 initially uses current limit +B from pin 18 to power internal drivers. These internal drivers amplify the oscillator signal and get out to pins 12 and 16. When the power supply stage works, the power comes for the bottom driver, VG(L); pin 12 from pin 10 (VC2) and for the top driver, VG(H); pin 16 from pin 14 (VB). The VB voltage is approximately +5V (average) above the reference voltage at IC6001/pin15.

Regulator Stage

This voltage supplies the top internal driver that amplifies the oscillator signal that leaves IC6001/pin 16. The regulating stage uses error detector IC6003 and optical isolator PH6001 to monitor the output from T6002. If the output is low, the voltage fed back to IC6001/pin 2 goes HIGH, decreasing the oscillator frequency. The decrease in frequency increases the output of T6002.

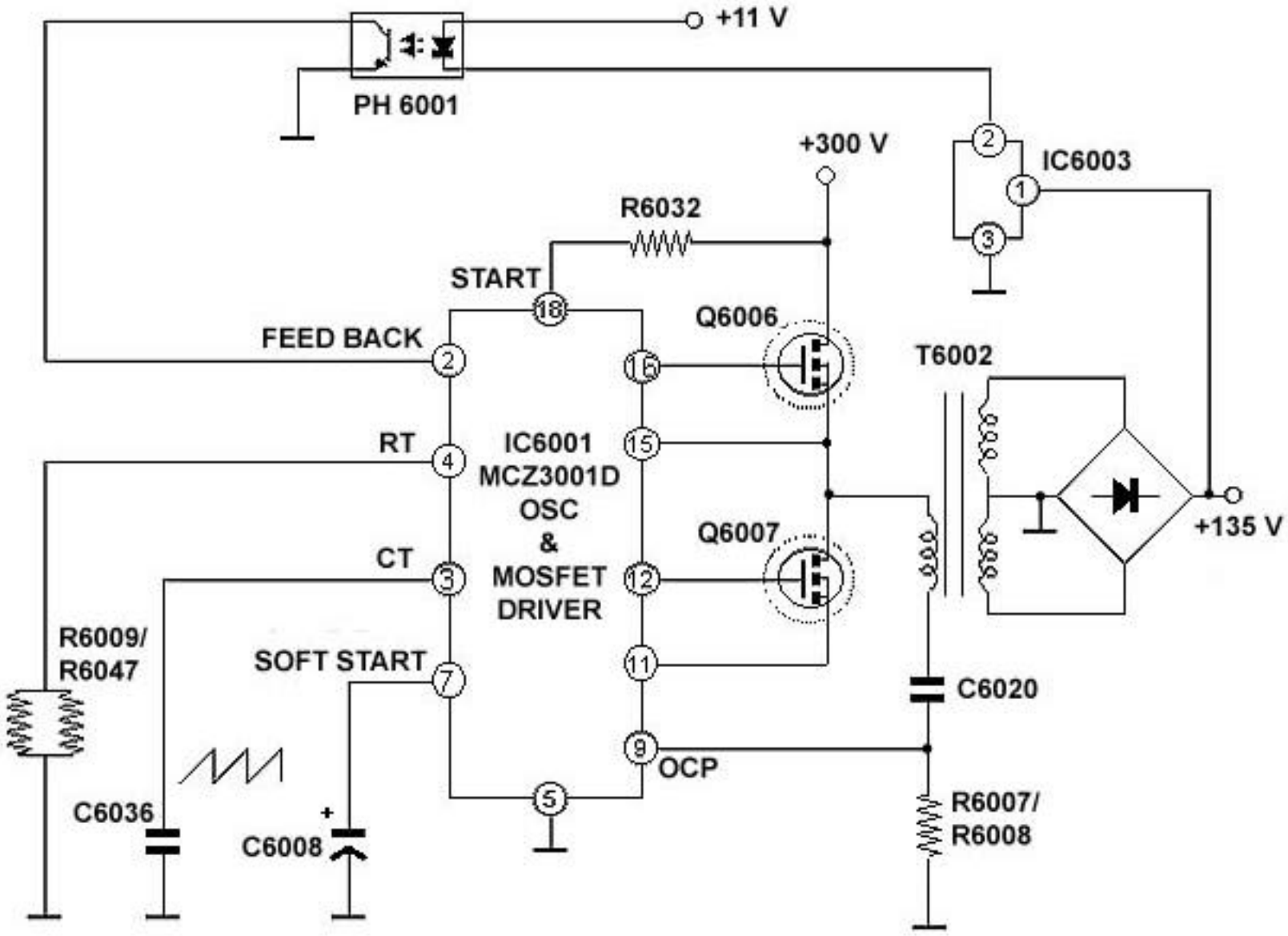


Figure 2.2 Main power supply circuit diagram.

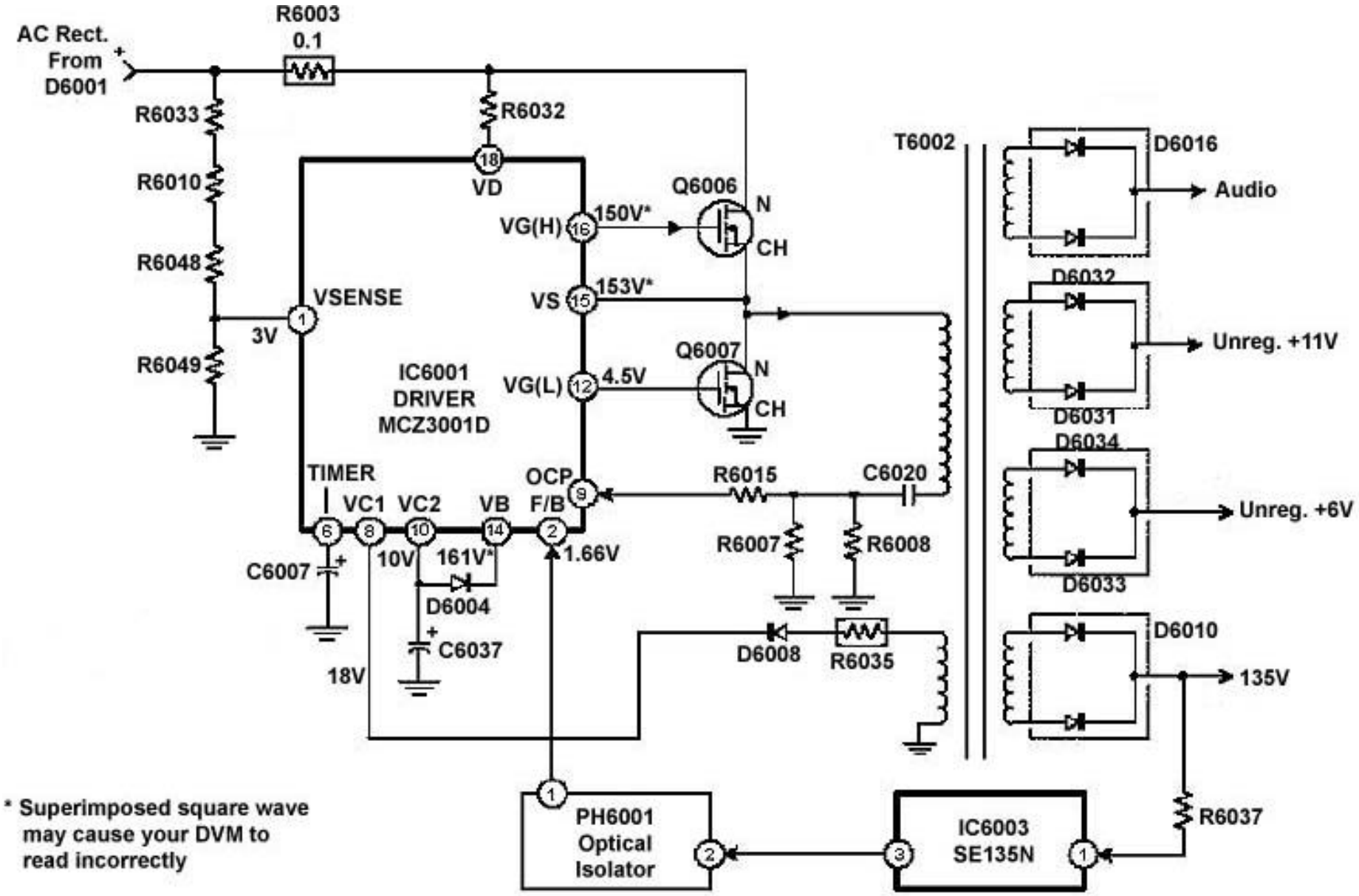


Figure 2.3 Main power supply circuit diagram.

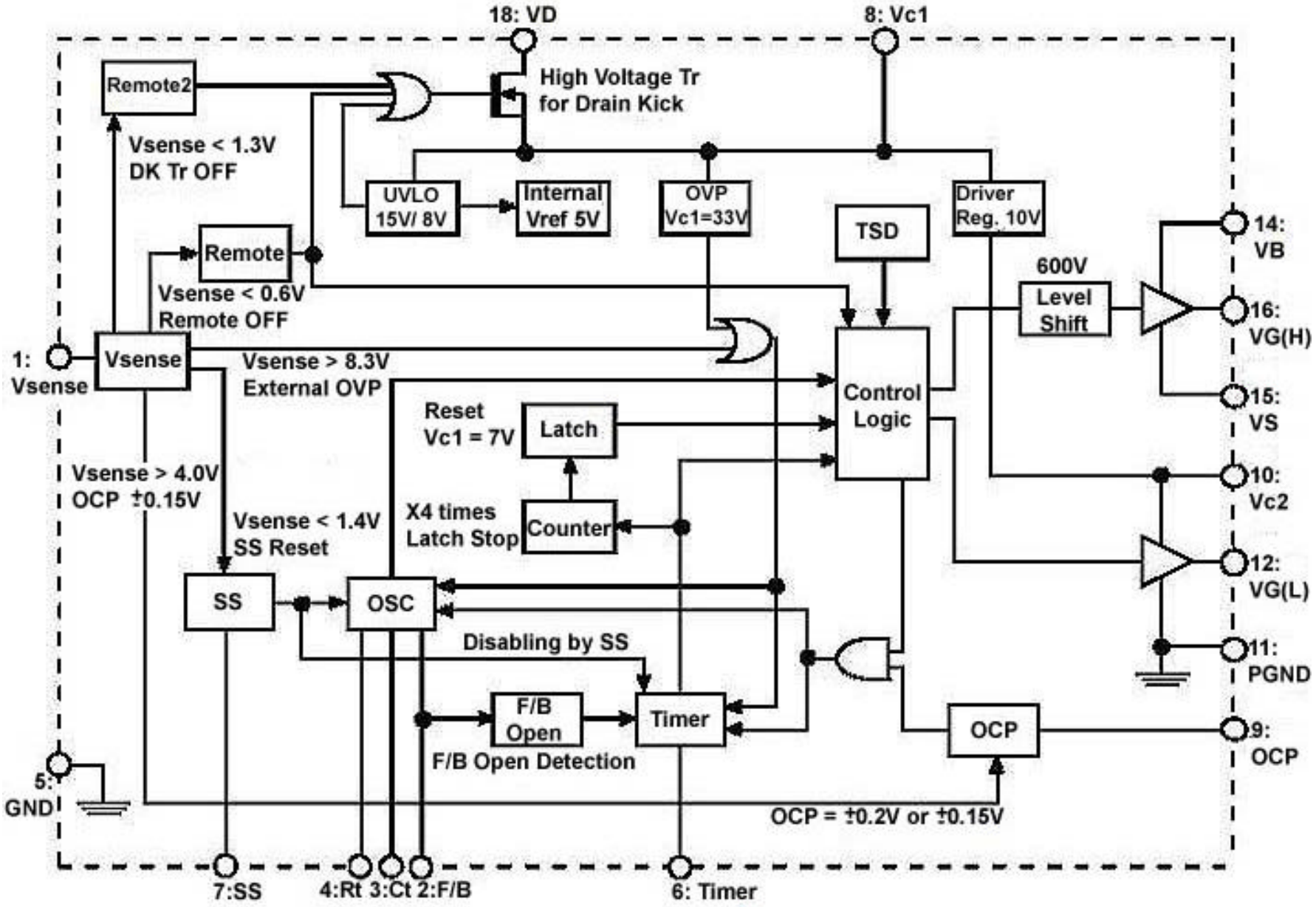


Figure 2.4 IC6001 block diagram.

2.3 Overvoltage Protection

With the voltage divider R6038, R6039 and R6040 the +B voltage is controlled. In case of failure, the zener diode D6009 is switched and a "high" signal is sent via resistor R6042 to pin 13 "OVP" at connector CN6006. Please refer to Figure 2.5

2.4 Overcurrent Protection

R6021 is the resistor to control the current on the +B line. If the voltage via R6021 goes to high the transistor Q6010 is switched. Then transistor Q6005 is switched and the error message "OCP" is at CN6006; Pin 12. Please refer to Figure 2.6

2.5 Protection Circuit of Power Block

- In case of OVP or OCP, the information goes to the A board via CN6006 and then direct via CN0001 to the micro controller on the M board pin 24 and pin 29.
- The main controller on the M board switch the main relay RY6001 on the G board and the TV set switch into standby.
- In case of OVP the LED flash three time.
- In case of OCP the LED flash two time to show the error to the outside.

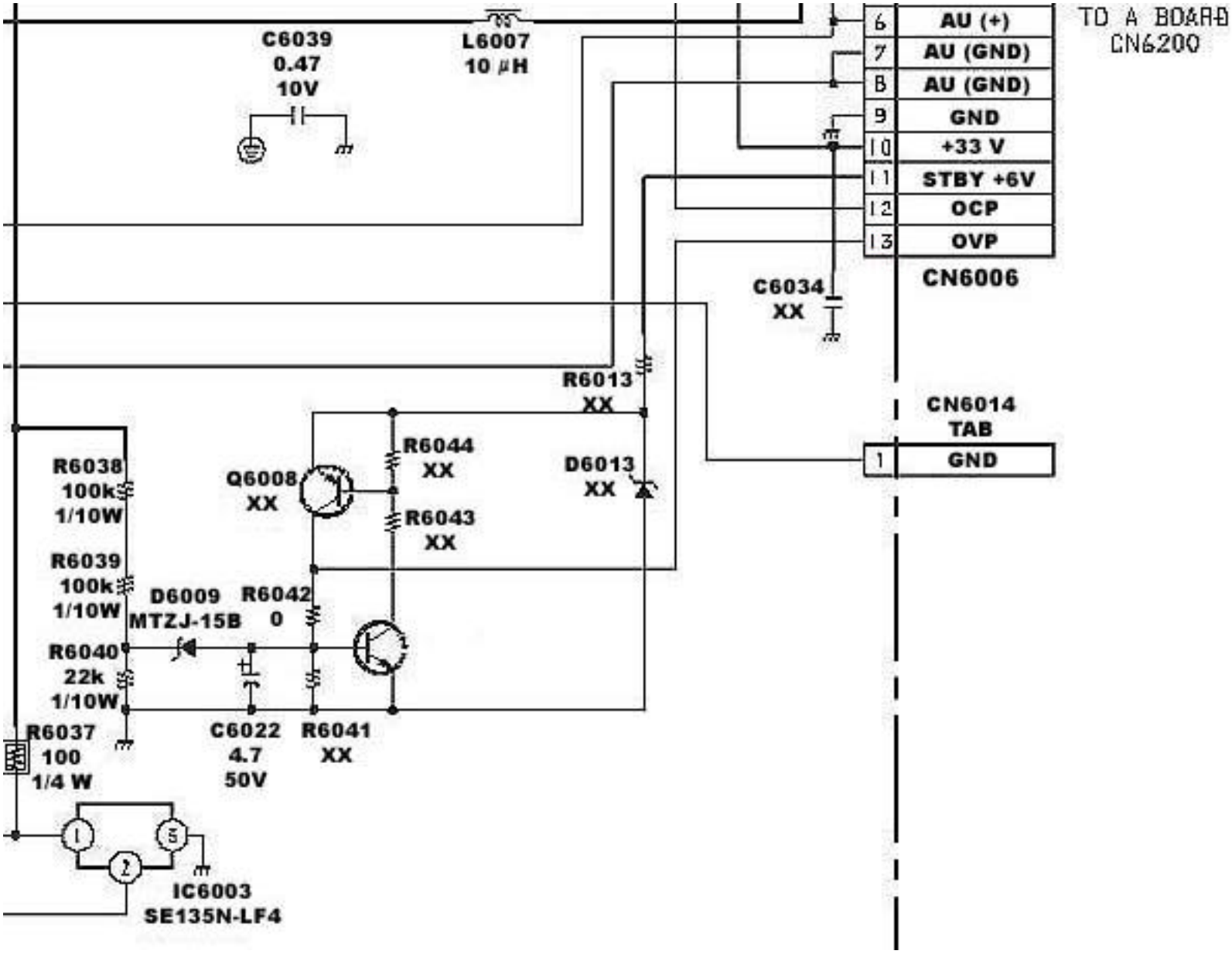


Figure 2.5
Overvoltage Protection

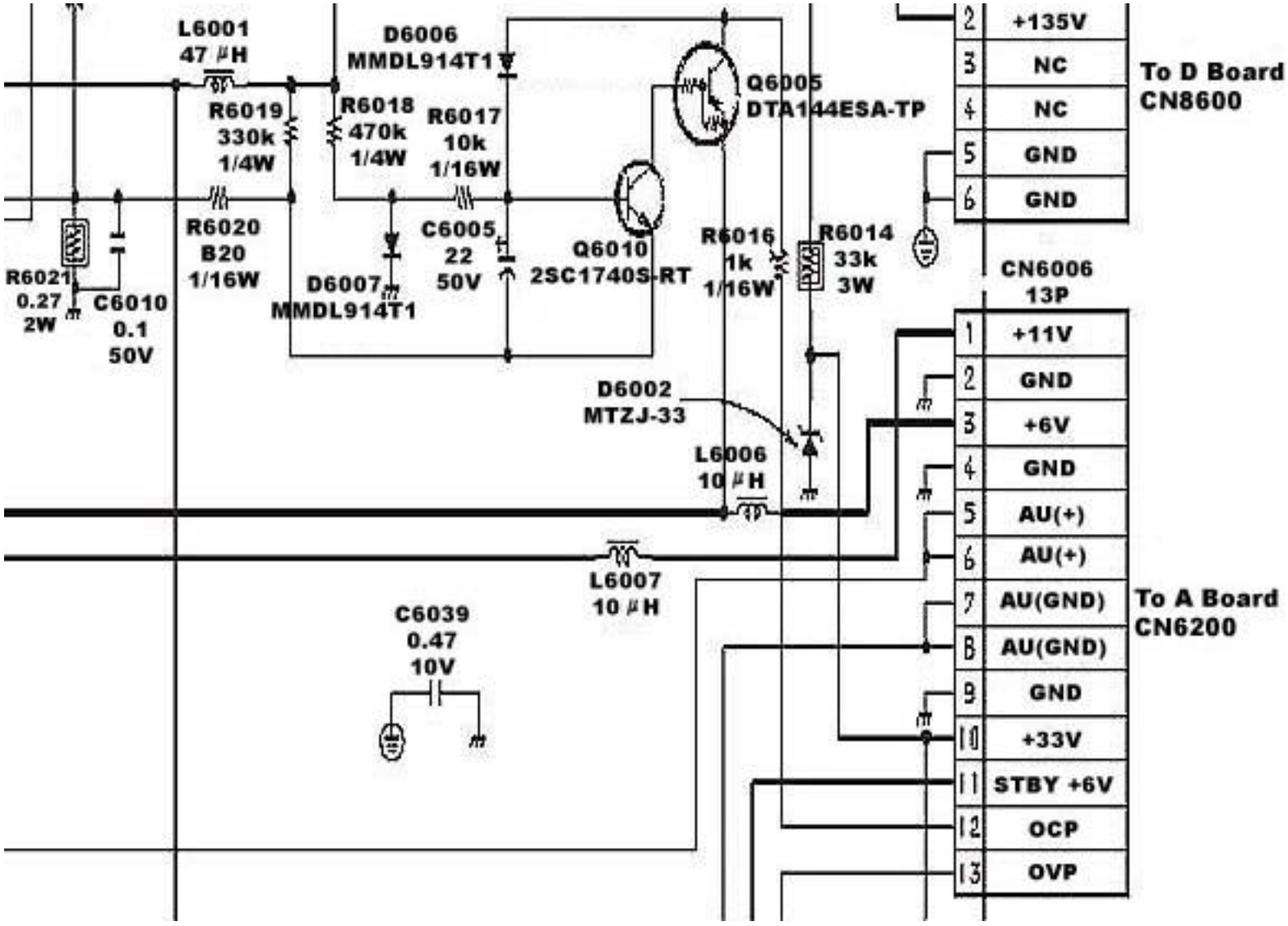
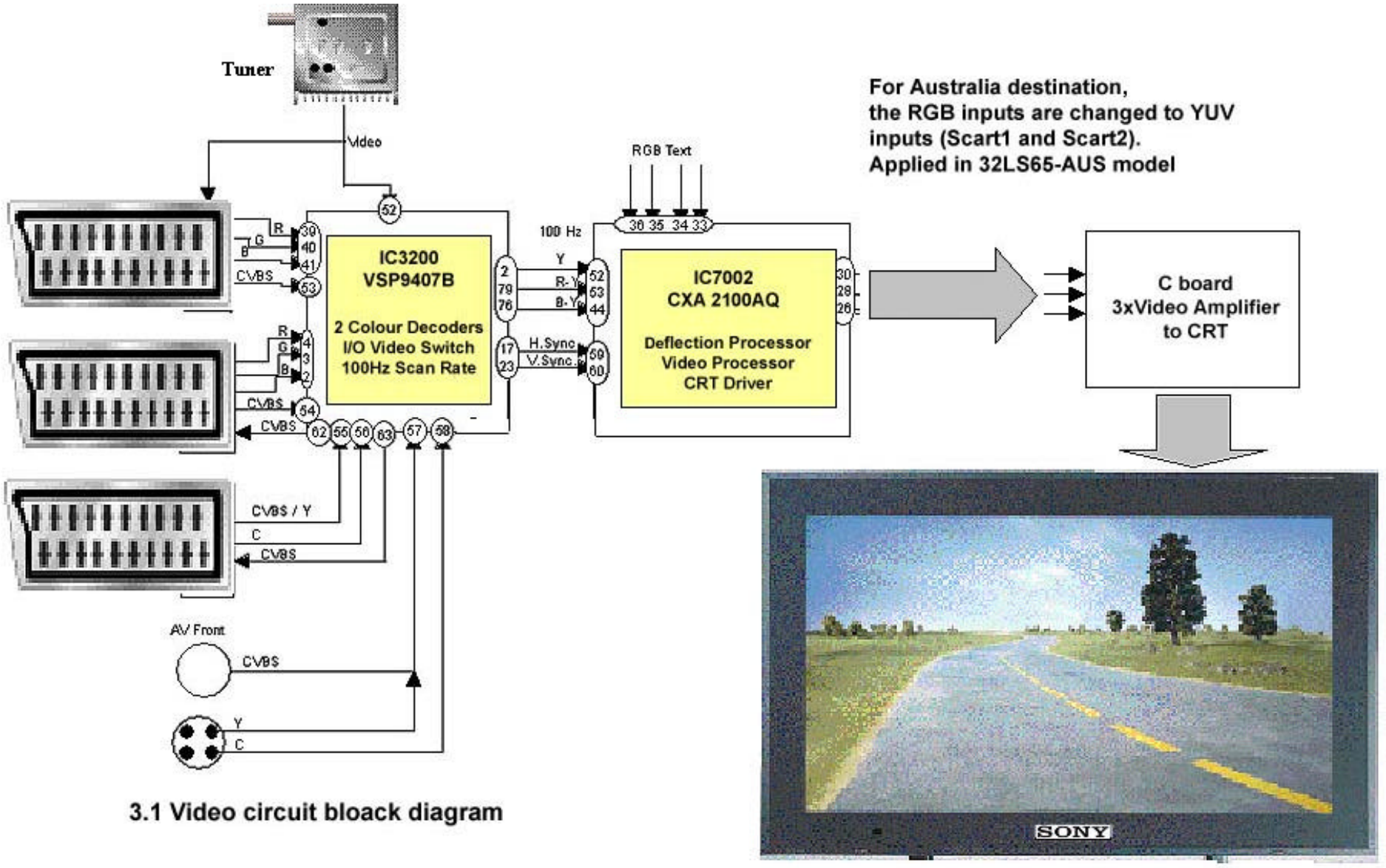


Figure 2.6
Overcurrent Protection

Chapter 3 Video Processing Circuit



3.1 Video circuit bloack diagram

3.1 VSP9407 Features

• Integrated Video Matrix switch
  – Up to 7 CVBS inputs and up to 2 Y/C inputs
  – Up to three CVBS outputs (even Y/C input)

• Multi-Standard colour decoder with 4H COMB FILTER
  – PAL/NTSC/SECAM -> Automatic recognition of chroma standard
  – 2 Colour Decoder: Main Channel + Picture in Picture
  – 2D COMB FILTER in the Main Channel.

• Detection embedded circuits:
  – Global motion and global still detection
  – Film mode and phase detection (PAL, NTSC; 2-2, 3-2 pull down)
  –Measurement of the noise level during the vertical retrace (blanking) for both channels
  – Detection of letter box formats

• Noise reduction:
  – Automatic measurement of the noise level
  – Motion adaptive temporal noise reduction
  – Intelligent Frame-based temporal noise reduction for luminance and chrominance, depending on both noise measured and motion detected pixel by pixel
  – Separate motion detection and noise measurement in both Master Channel (Main Picture) and Slave Channel (PIP)

• Scan-rate-conversion:
  – Motion adaptive frame based 100/120Hz interlaced scan conversion.
  – Special treatment for film material ('Inverse 3-2 pull down')
  – Large area flicker and line flicker reduction.
  – Simple Interlaced Modes (100/120Hz):
    a) ABAB, if still picture (avoiding line flicker)
    b) AA'B'B, if moving picture (avoiding artefacts)
    c) AAAA or BBBB, for Teletext (avoiding line flicker)
    d) Sharpness improvement
  – Digital colour transition improvement (DCTI)
  – Digital luminance transition improvement (DLTI)
  – Adaptive horizontal and vertical PEAKING (luminance)

• Three D/A converters:
  – 9 bit amplitude resolution for Y, -(R-Y), -(B-Y) output

Figure 3.2 shows the block diagram of VSP9407 while Figure 3.3 shows its pinning diagram.

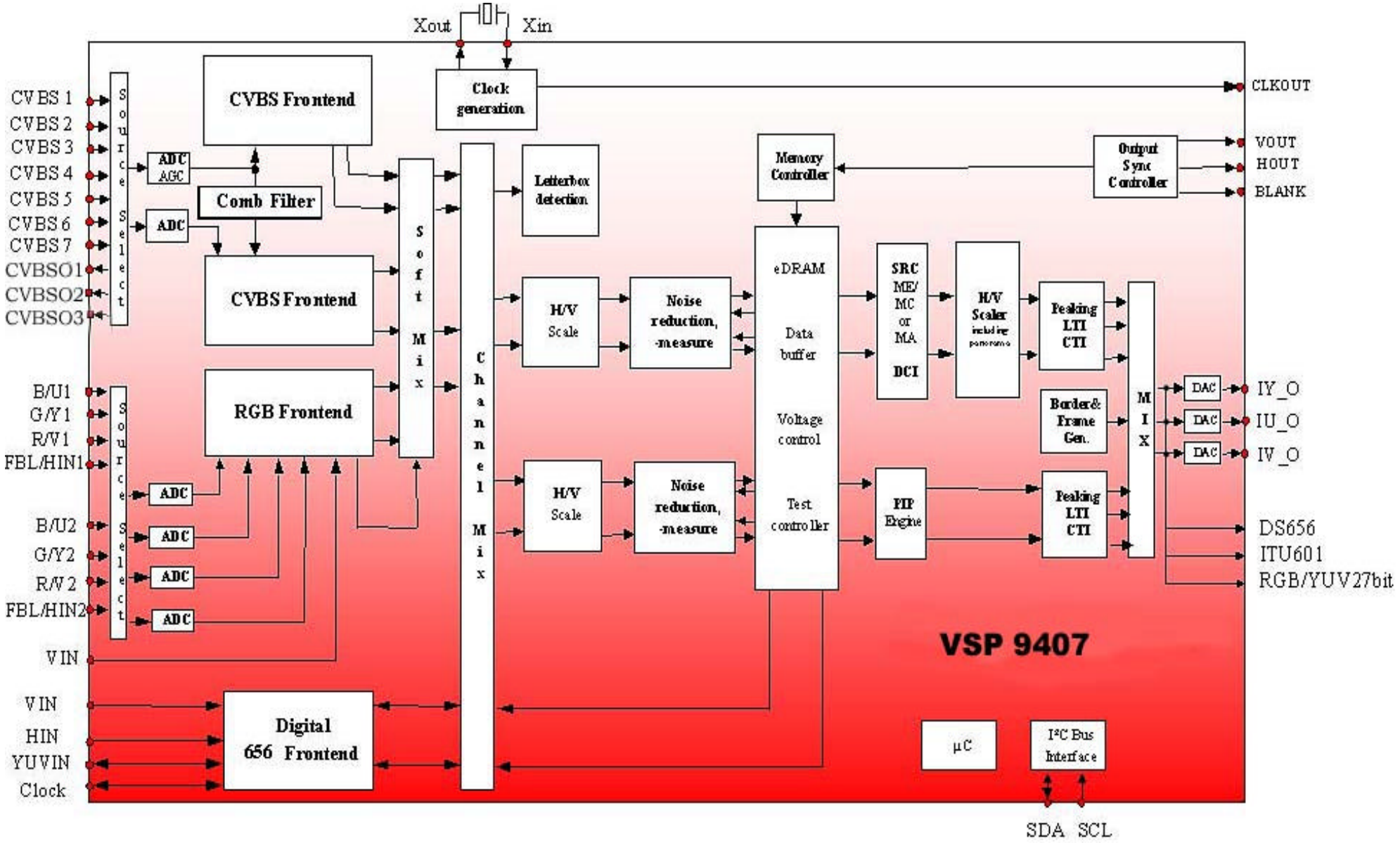


Figure 3.2 VSP 9407 Block Diagram

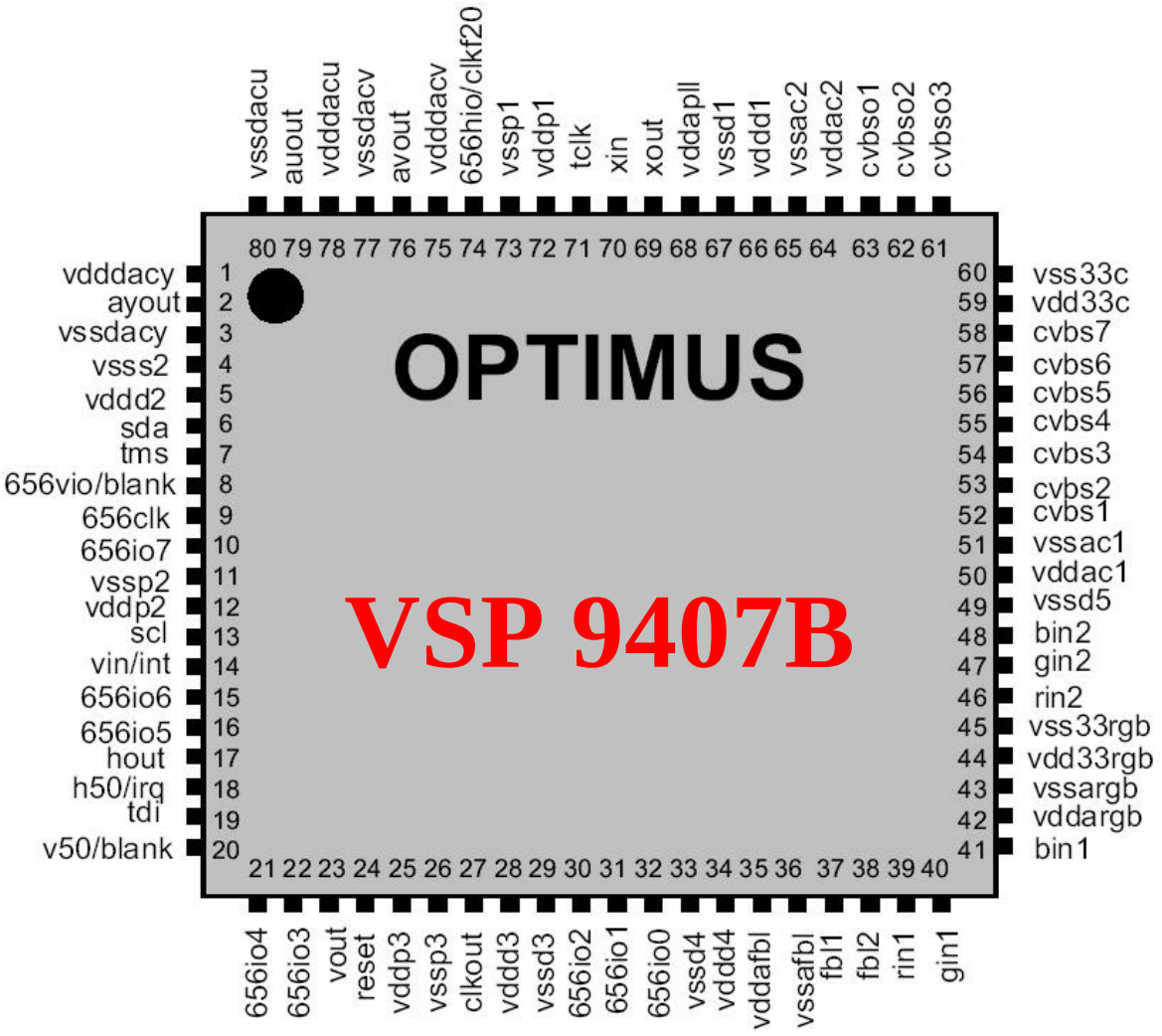


Figure 3.3 VSP9407 Pinning

3.2 Features of CRT Driver (CXA 2100)

- Two sets of switchable YCbCr input
- CbCr input offset adjustment circuit
- LTI and CTI circuits
- AKB system
- Two sets of analog RGB inputs
- Horizontal sync processing that supports 31.5kHz
- Vertical deflection circuit that supports 50/60/100/120Hz
- Deflection compensation circuit capable of supporting various wide modes
- H drive soft start/ stop function

Figure 3.4 shows CXA 2100 pinning diagram while Figure 3.5 shows its block diagram.

Figure 3.4 CXA 2100 Pinning Diagram

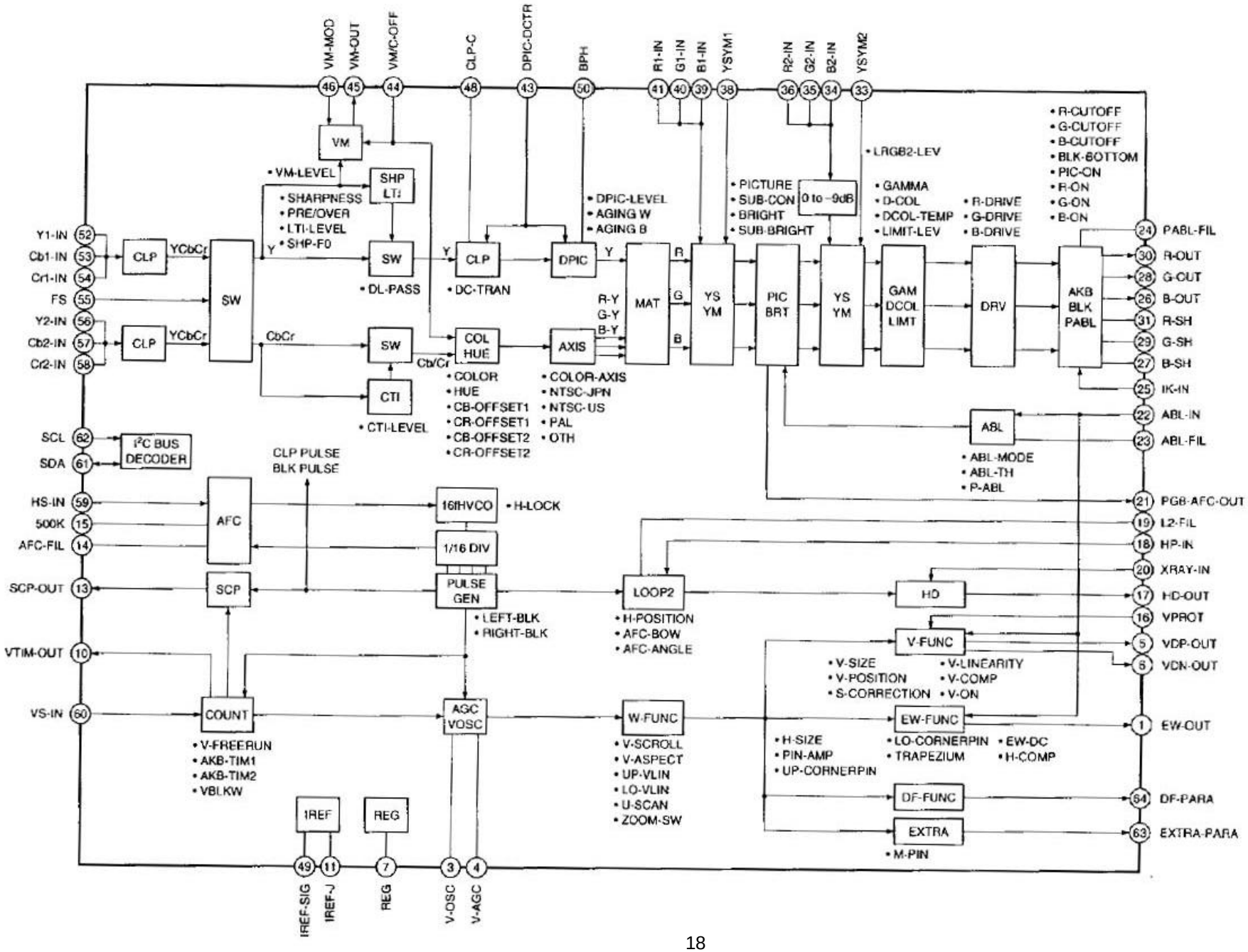


Figure 3.5

CXA 2100 Block Diagram

Chapter 4 Micro Controller

4.1 Features of SAA5667 Micro Controller

SAA5667 is a single-chip microcontroller based on 80C51 microcontroller, which is integrated with On-Screen Display (OSD) and Data Capture and display function for Teletext.

It has 32 I/O ports via individual addressable controls, which are 5 V tolerant digital inputs and I/O. There are two port lines with 8 mA sink for direct drive of LED. The byte level I²C-bus up to 400 kHz dual port I/O.

Besides, SAA5667 has large Character ROM that allows up to 1020 characters of 12 * 10 pixels. There are 64 Characters for OSD.

There is a single crystal oscillator for micro-controller, OSD and data capture. The power reduction mode will be Idle, Standby and Power down.

Figure 4.1 shows the block diagram of SAA5667.

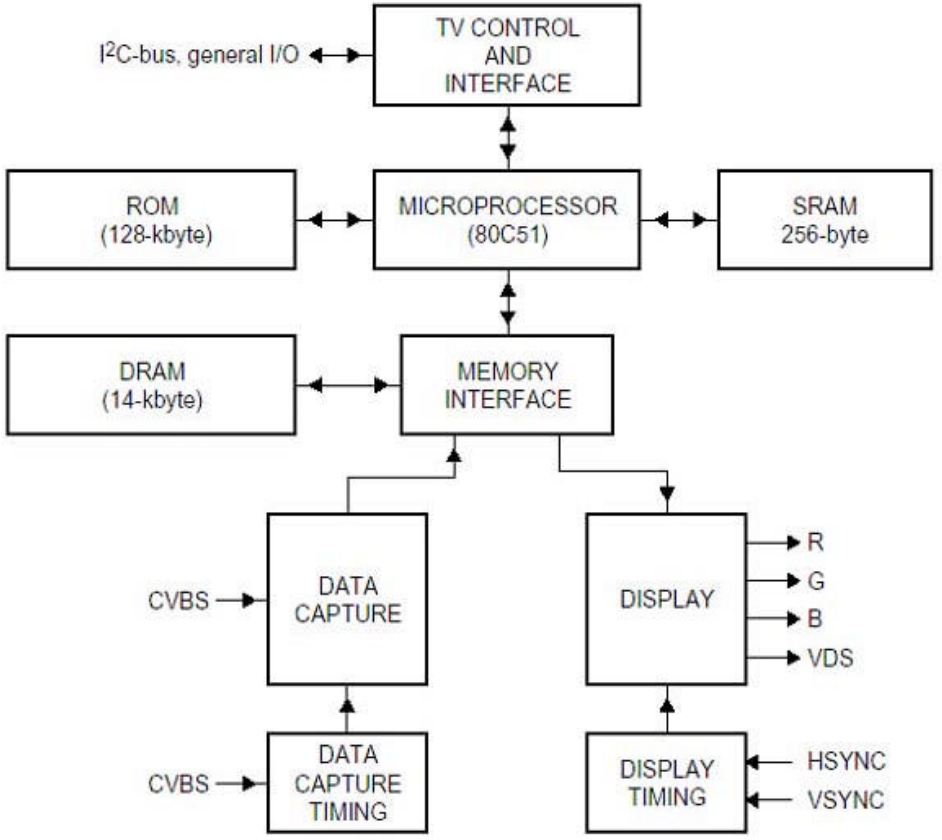


Figure 4.1 SAA5667 block diagram.

Chapter 5 Audio Circuit

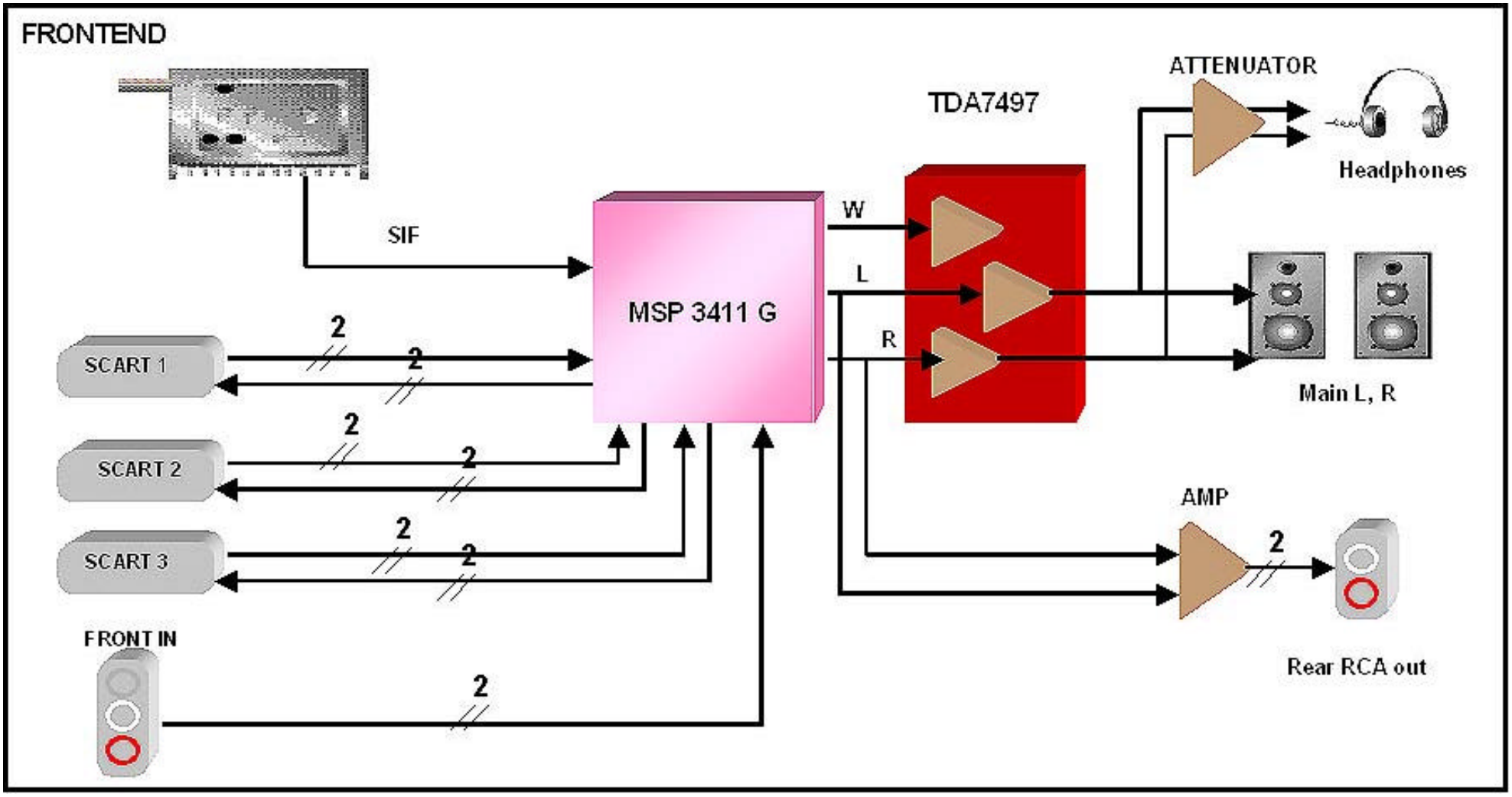


Figure 5.1 Audio block diagram for AE-6B chassis

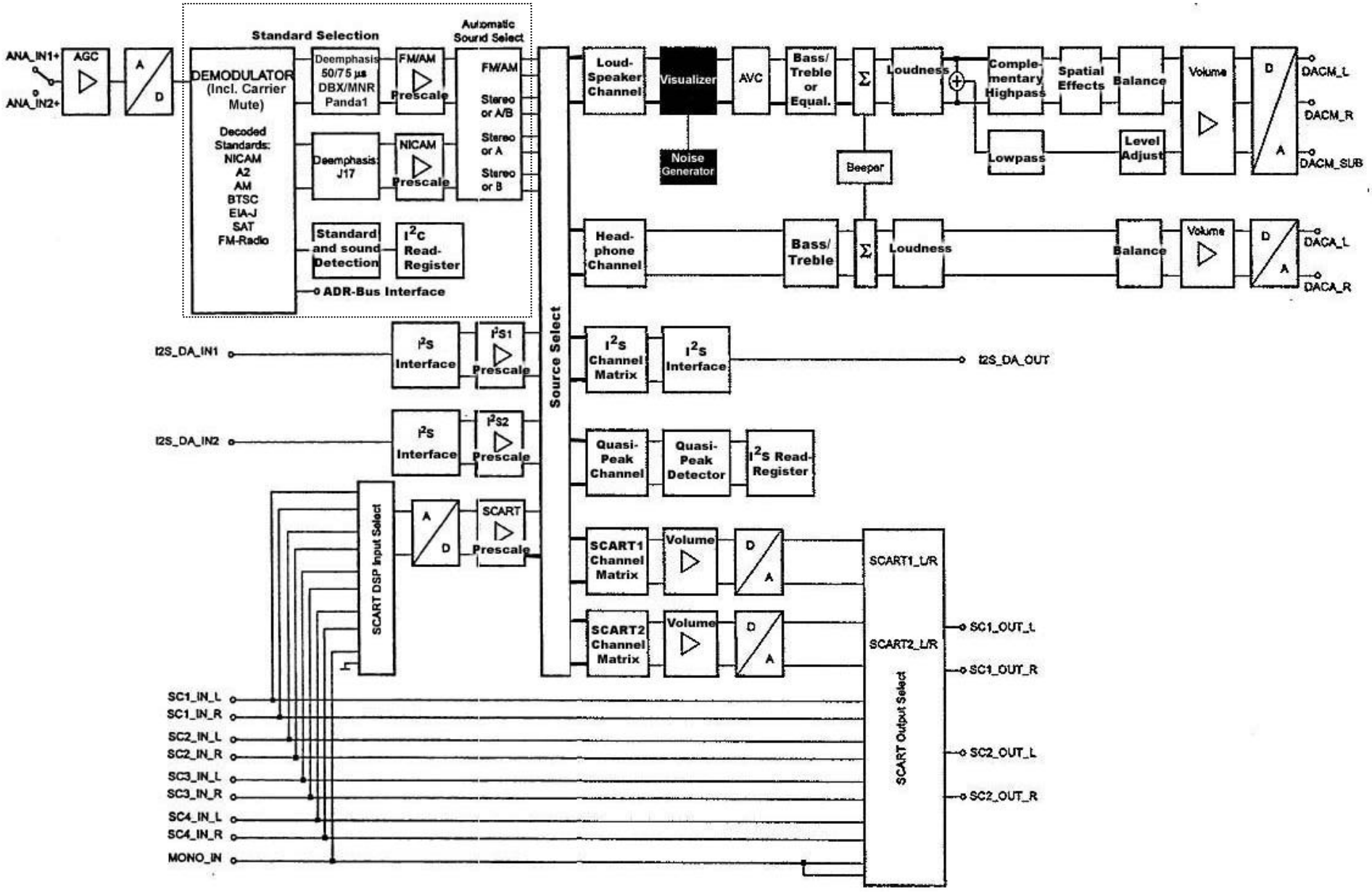


Figure 5.2 MSP3411G block diagram

5.1 Features of MSP3411G-B9

MSP3411G-B9 is a multistandard sound processor. It enables **Virtual Dolby Surround** and **BBE Digital Sound**. It has 4 to 2 stereo matrix switching facilities. Besides, it has tone and balance controls as well as Automatic Volume Correction for loudspeaker channel. Figure 5.2 shows the block diagram of MSP3411G.

5.2 Features of TDA7497 Triple Amplifier

Figure 5.3 shows the pin diagram of TDA7497 while Figure 5.4 shows its block diagram. It is a 10W + 10 W + 18W amplifier that has Independent Mute for centre channel and main channel. There is no Turn-on Turn-off Pop Noise. Besides, there is protection for short circuit and thermal overload.

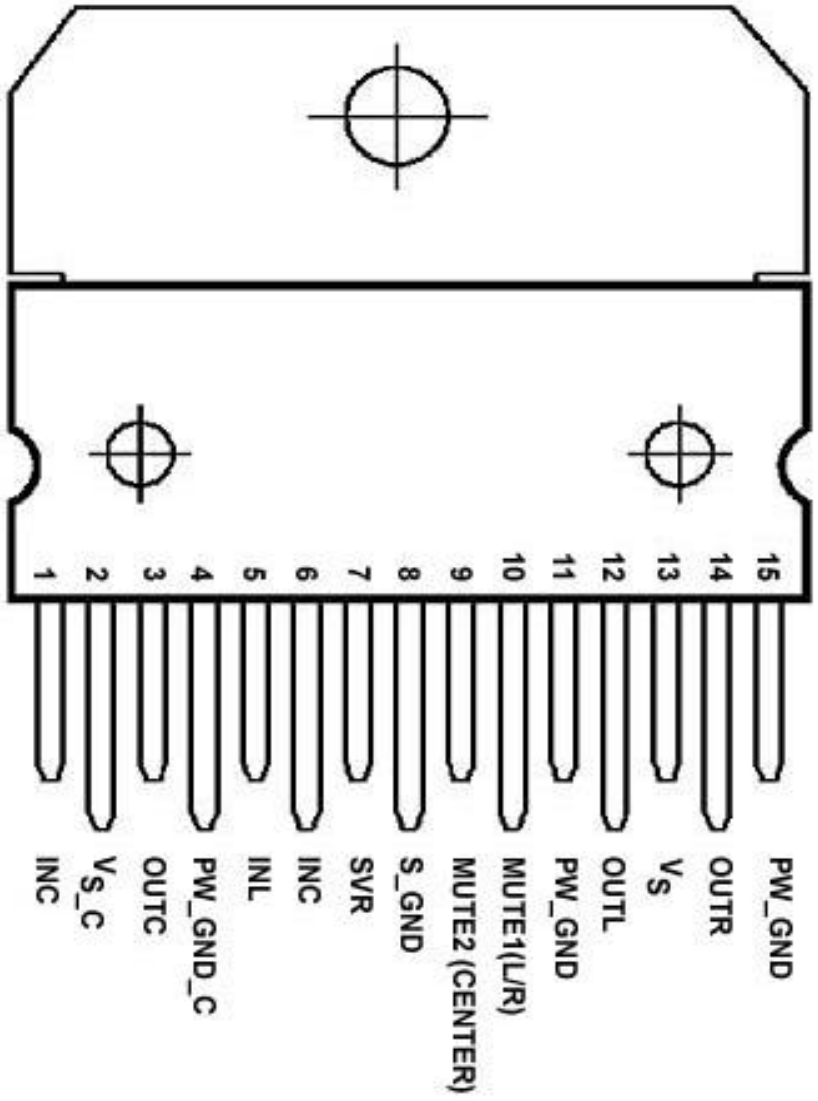


Figure 5.3 Pin diagram of TDA7497

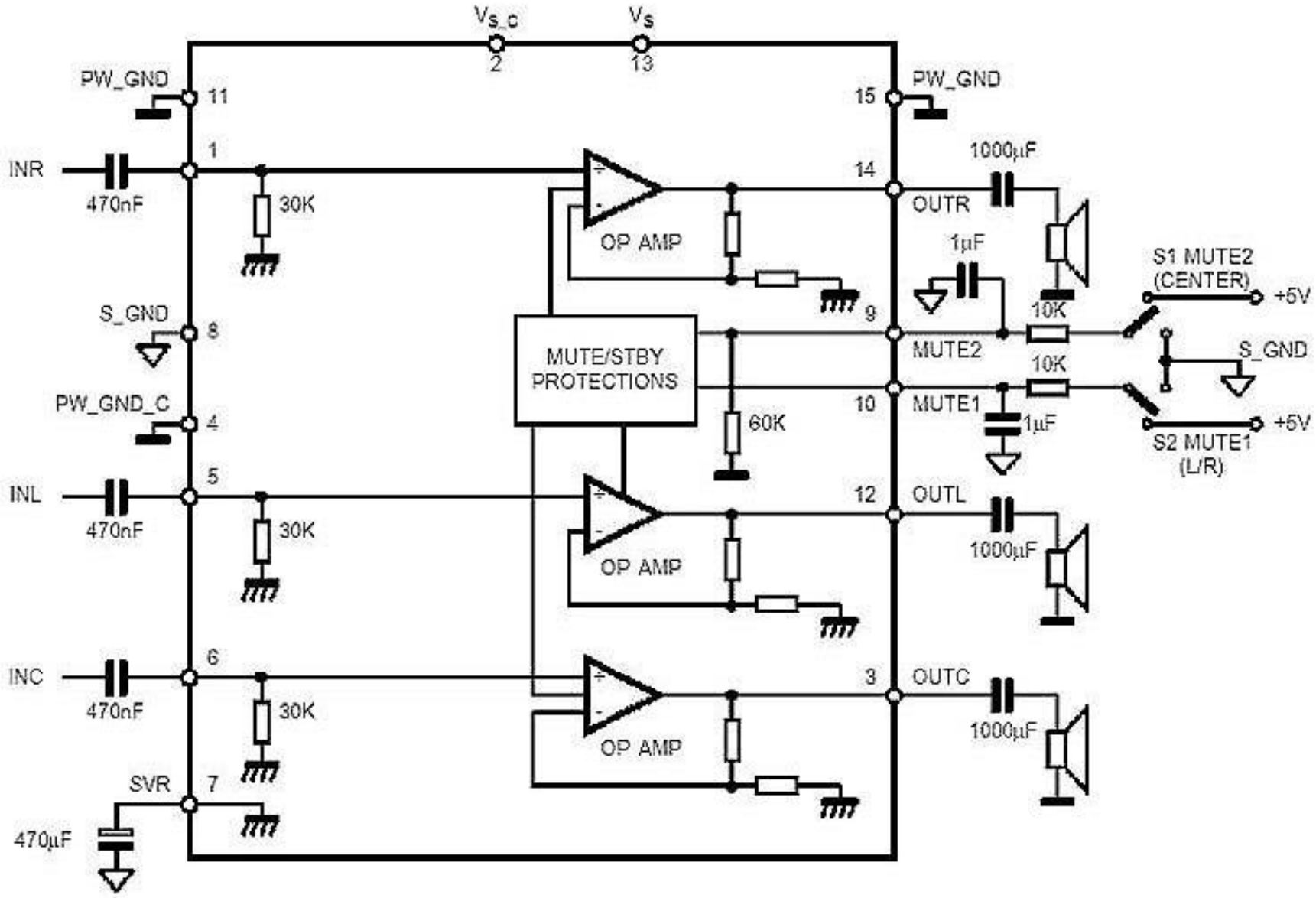
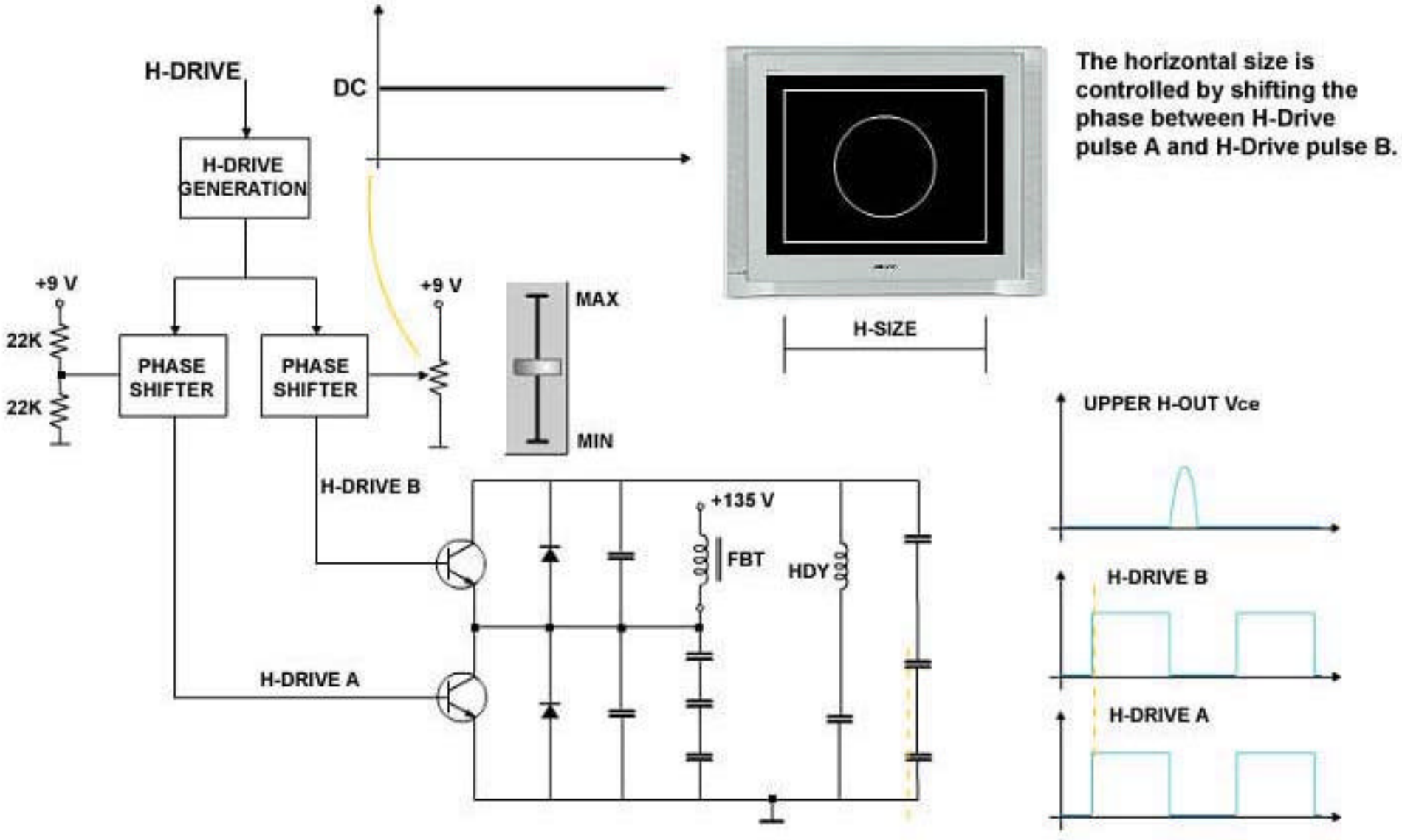
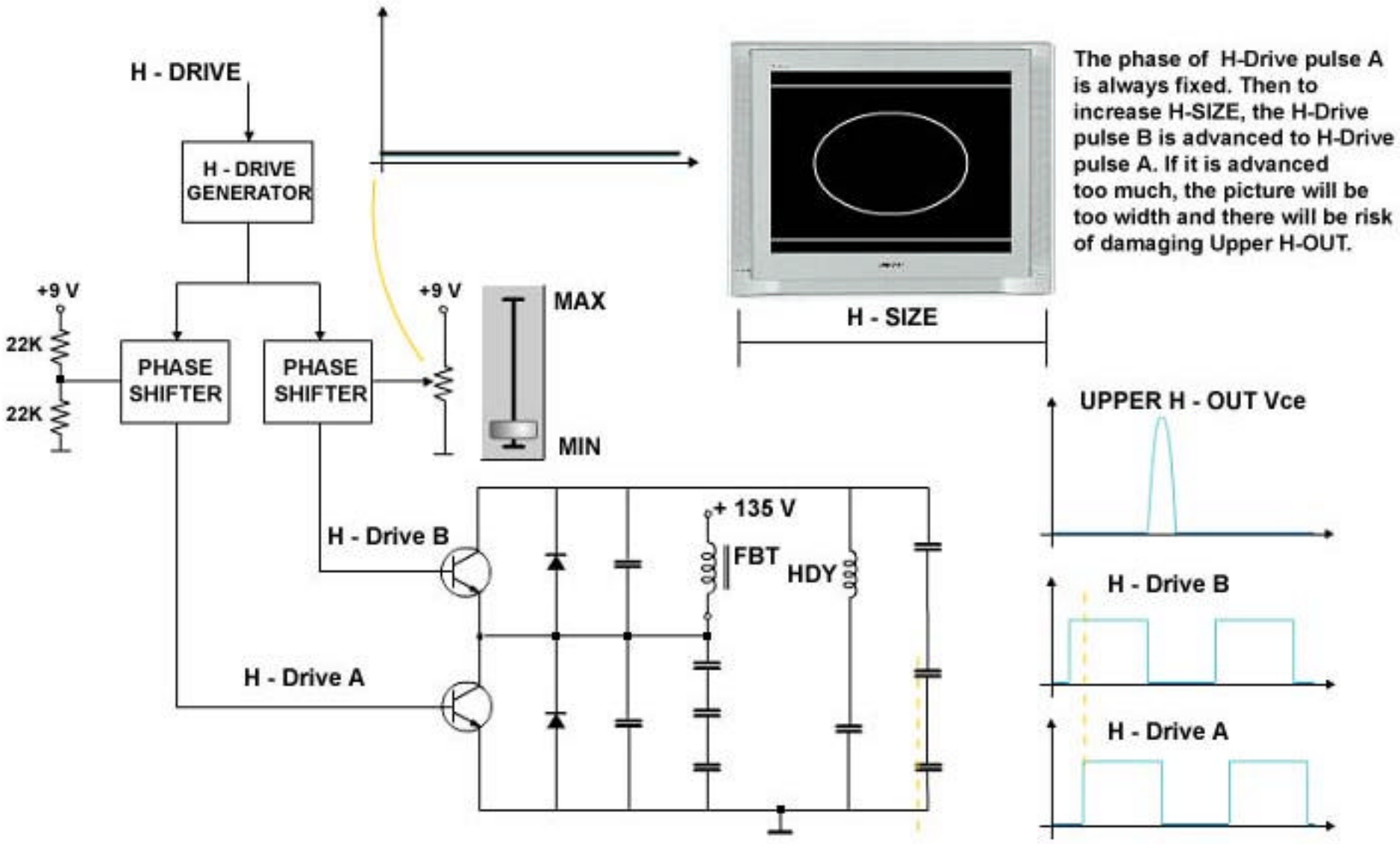
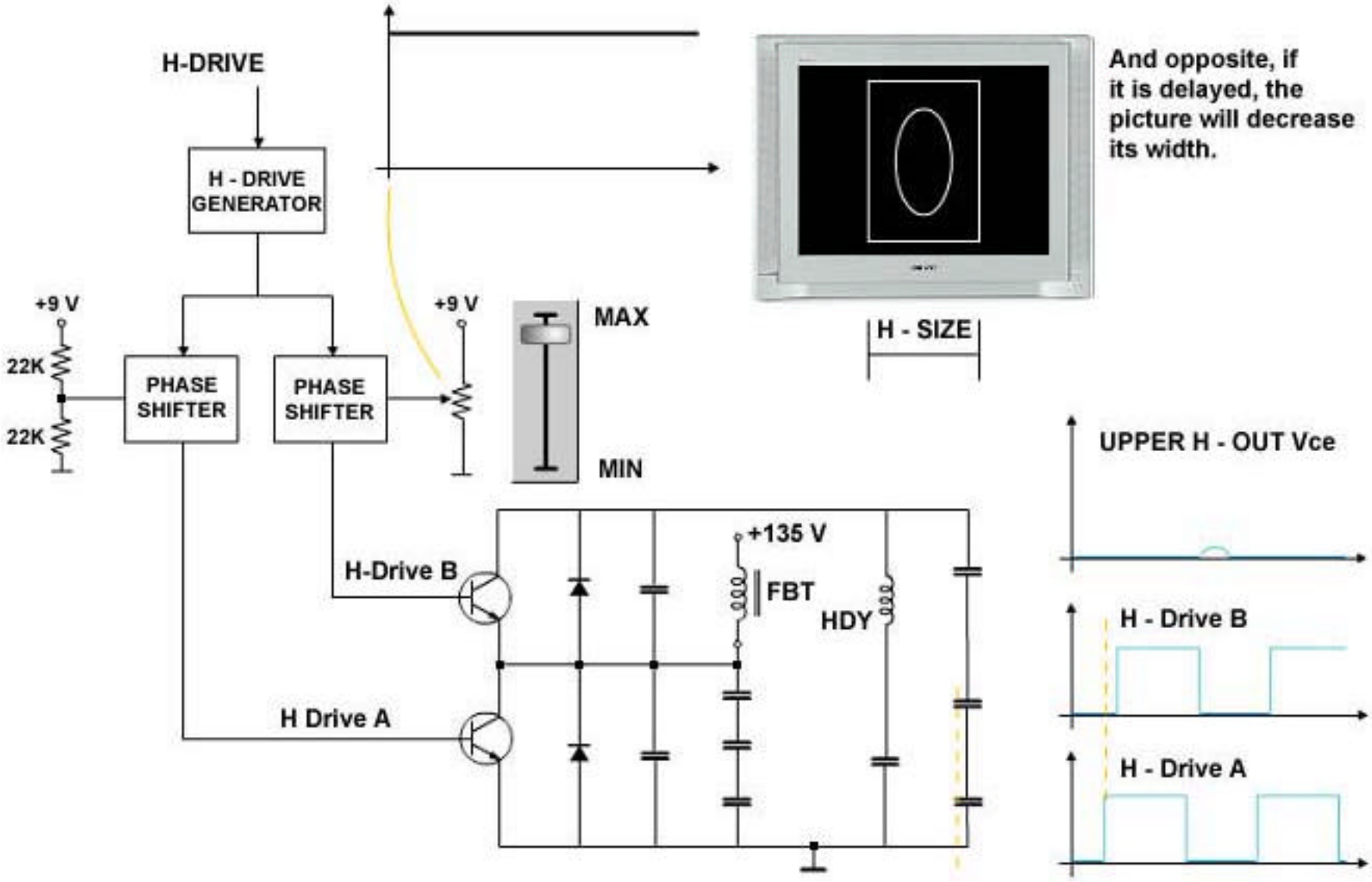


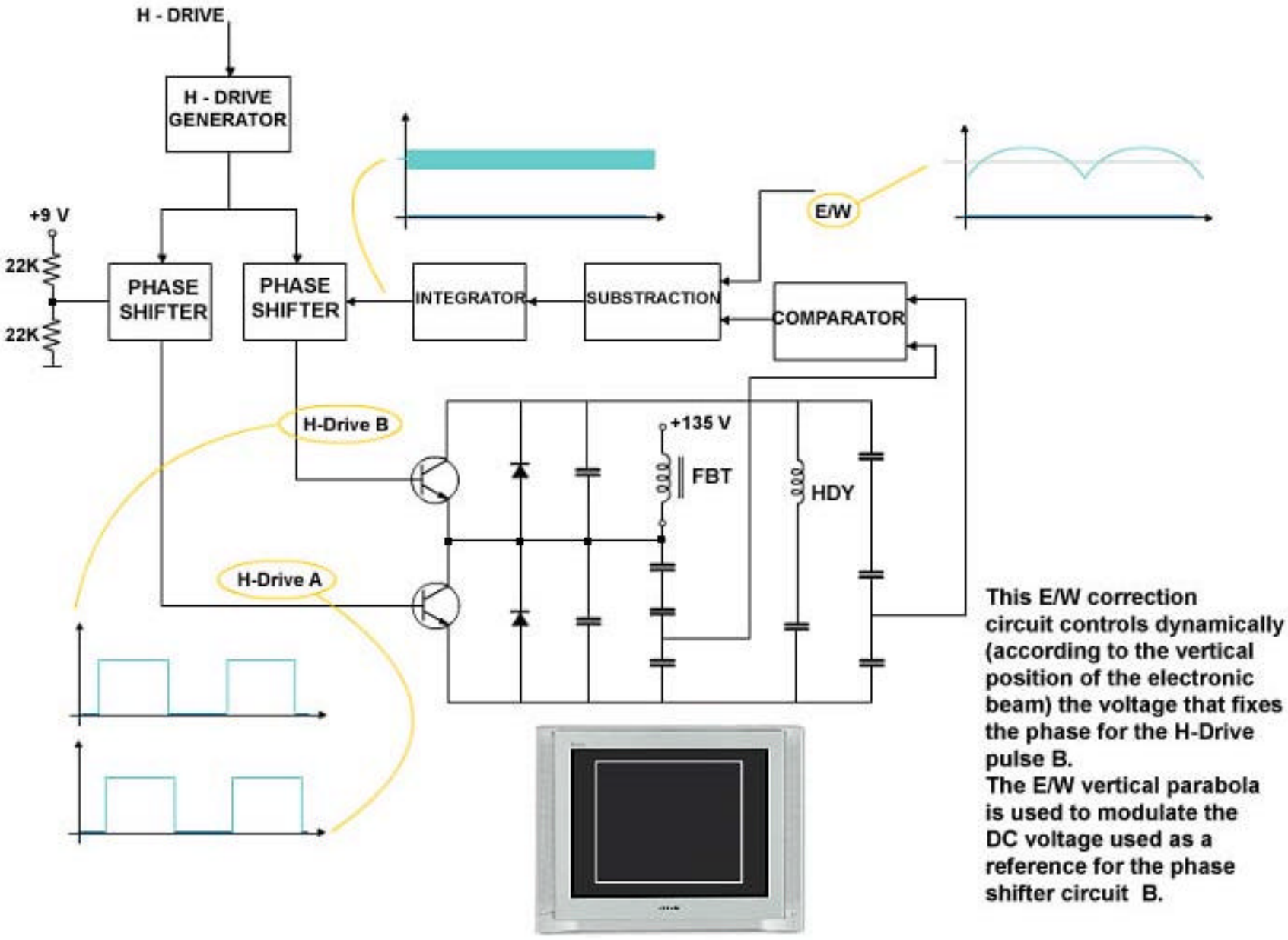
Figure 5.4 TDA7497 block diagram

Chapter 6 Deflection Circuit

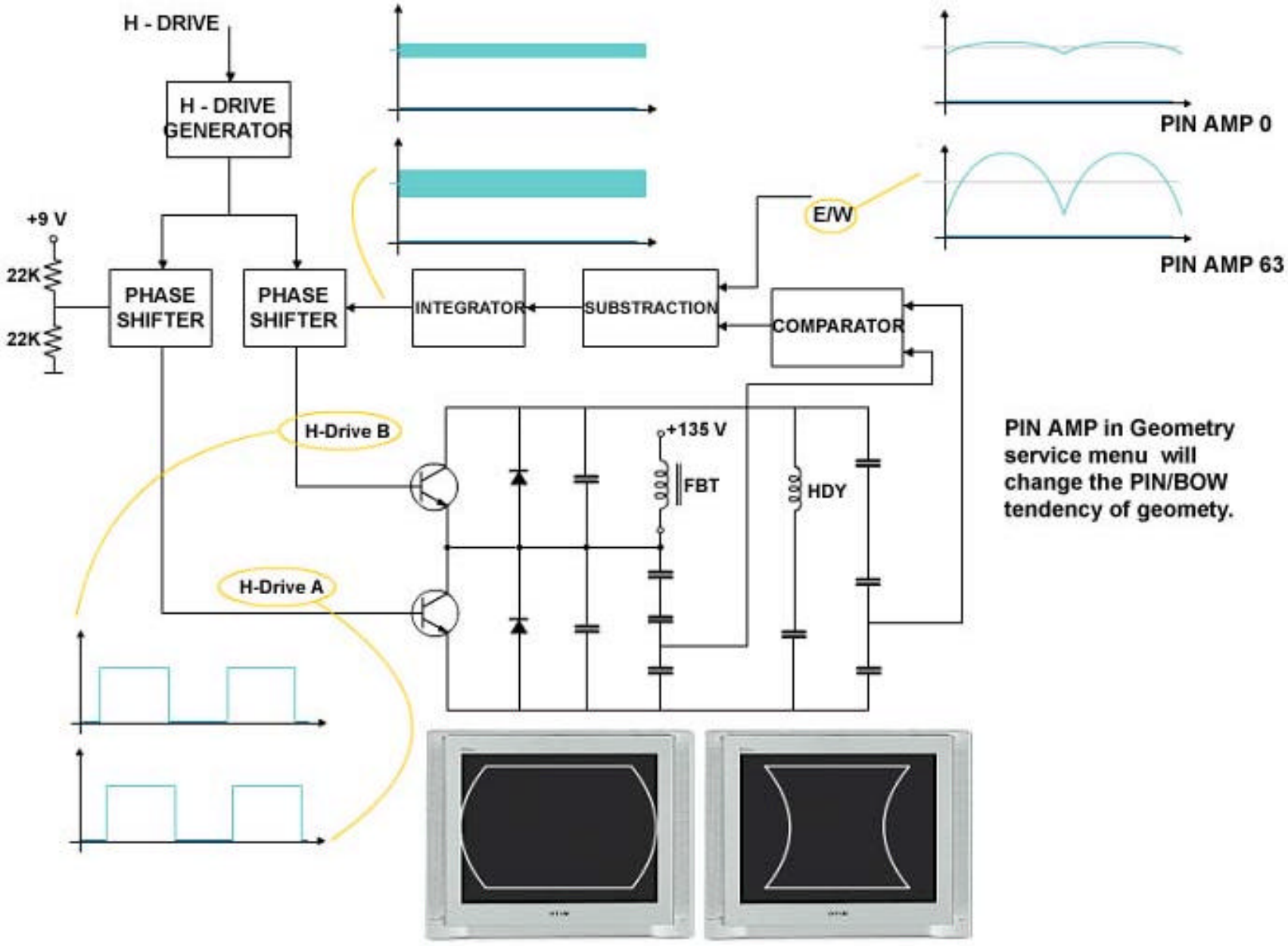



H - DRIVE
H - DRIVE GENERATOR
+9 V
22K
22K
PHASE SHIFTER
PHASE SHIFTER
+9 V
MAX
MIN
H - SIZE
The phase of H-Drive pulse A is always fixed. Then to increase H-SIZE, the H-Drive pulse B is advanced to H-Drive pulse A. If it is advanced too much, the picture will be too width and there will be risk of damaging Upper H-OUT.
H - Drive B
H - Drive A
+ 135 V
FBT
HDY
UPPER H - OUT Vce
H - Drive B
H - Drive A

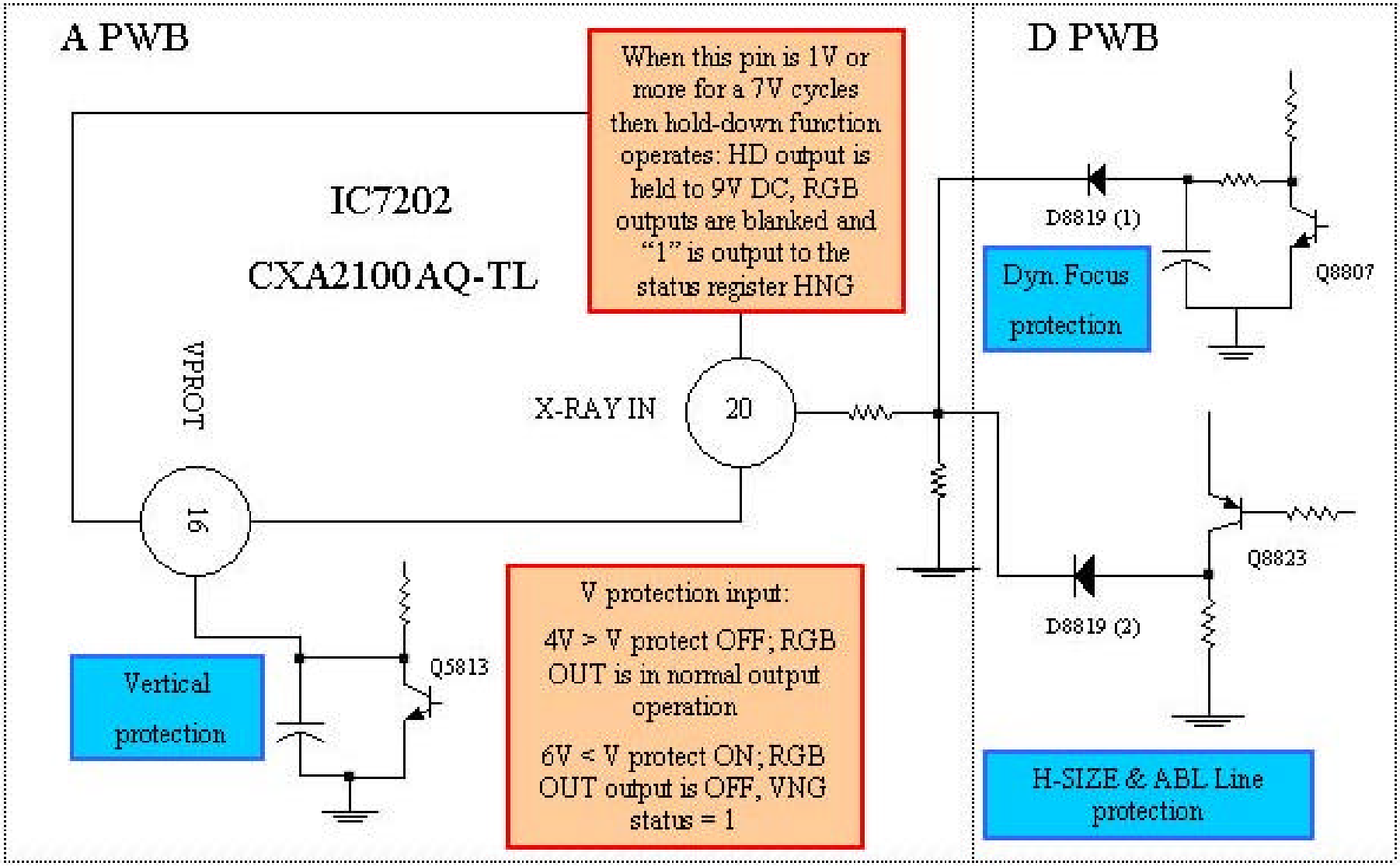

H-DRIVE
H - DRIVE GENERATOR
+9 V
22K
22K
PHASE SHIFTER
PHASE SHIFTER
+9 V
MAX
MIN
H - SIZE
And opposite, if it is delayed, the picture will decrease its width.
+135 V
FBT
HDY
H-Drive B
H Drive A
UPPER H - OUT Vce
H - Drive B
H - Drive A



This E/W correction circuit controls dynamically (according to the vertical position of the electronic beam) the voltage that fixes the phase for the H-Drive pulse B.
The E/W vertical parabola is used to modulate the DC voltage used as a reference for the phase shifter circuit B.


H - DRIVE
H - DRIVE GENERATOR
+9 V
22K
22K
PHASE SHIFTER
PHASE SHIFTER
INTEGRATOR
SUBSTRACTION
COMPARATOR
E/W
PIN AMP 0
PIN AMP 63
H-Drive B
H-Drive A
+135 V
FBT
HDY
PIN AMP in Geometry service menu will change the PIN/BOW tendency of geomety.

6.1 Deflection Block AE-6B (Protections)



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