4510B

UP/DOWN DECADE COUNTER

DESCRIPTION – The 4510B is an Edge-Triggered Synchronous Up/Down BCD Counter with a Clock Input ($\overline{CP}$), an active HIGH Up/Down Count Control Input (Up/$\overline{Dn}$), an active LOW Count Enable Input ($\overline{CE}$), an asynchronous active HIGH Parallel Load Input (PL), four Parallel Inputs (P_0-P_3), four Parallel Outputs (Q_0-Q_3), an active LOW Terminal Count Output ($\overline{TC}$) and an overriding asynchronous Master Reset Input (MR).

Information on the Parallel Inputs (P_0-P_3) is loaded into the counter while the Parallel Load Input (PL) is HIGH, independent of all other input conditions except the Master Reset Input (MR) which must be LOW. With the Parallel Load Input (PL) LOW, the counter changes on the LOW-to-HIGH transition of the Clock Input (CP) if the Count Enable Input ($\overline{CE}$) is LOW. The Up/Down Count Control Input (Up/$\overline{Dn}$) determines the direction of the count, HIGH for counting up, LOW for counting down. When counting up, the Terminal Count Output ($\overline{TC}$) is LOW when the Parallel Outputs Q_0-Q_3 are HIGH and the Count Enable ($\overline{CE}$) is LOW. When counting down, the Terminal Count Output ($\overline{TC}$) is LOW when all the Parallel Outputs (Q_0-Q_3) and the Count Enable Input ($\overline{CE}$) are LOW. A HIGH on the Master Reset Input resets the counter (Q_0-Q_3 = LOW) independent of all other input conditions.

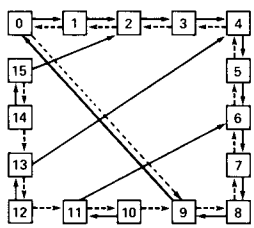
- **UP/DOWN COUNT CONTROL**
- **SINGLE CLOCK INPUT (L→H EDGE-TRIGGERED)**
- **ASYNCHRONOUS PARALLEL LOAD INPUT**
- **ASYNCHRONOUS MASTER RESET**
- **EASILY CASCADABLE**

MODE SELECTION TABLE

PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
H	X	X	X	Parallel Load ($P_n \rightarrow Q_n$)
L	X	H	X	No Change
L	L	L	⎍	Count Down, Decade
L	H	L	⎍	Count Up, Decade

MR = LOW
H = HIGH Level
L = LOW Level
X = Don't Care
⎍ = Positive-Going Transition

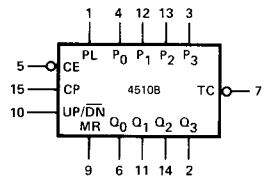
4510B STATE DIAGRAM



LOGIC EQUATION FOR TERMINAL COUNT

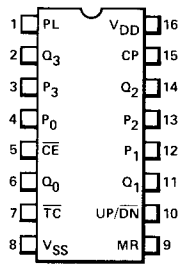
$TC = CE \bullet [(UP \bullet Q_0 \bullet Q_3) + (\overline{UP} \bullet \overline{Q}_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet \overline{Q}_3)]$

LOGIC SYMBOL



V_{DD} = Pin 16
V_{SS} = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pin-outs (Connection Diagram) as the Dual In-line Package.

PIN NAMES

PL	Parallel Load Input (Active HIGH)
P_0-P_3	Parallel Inputs
$\overline{CE}$	Count Enable Input (Active LOW)
CP	Clock Pulse Input (L → H Edge-Triggered)
Up/$\overline{Dn}$	Up/Down Count Control Input
MR	Master Reset Input
$\overline{TC}$	Terminal Count Output (Active LOW)
Q_0-Q_3	Parallel Outputs

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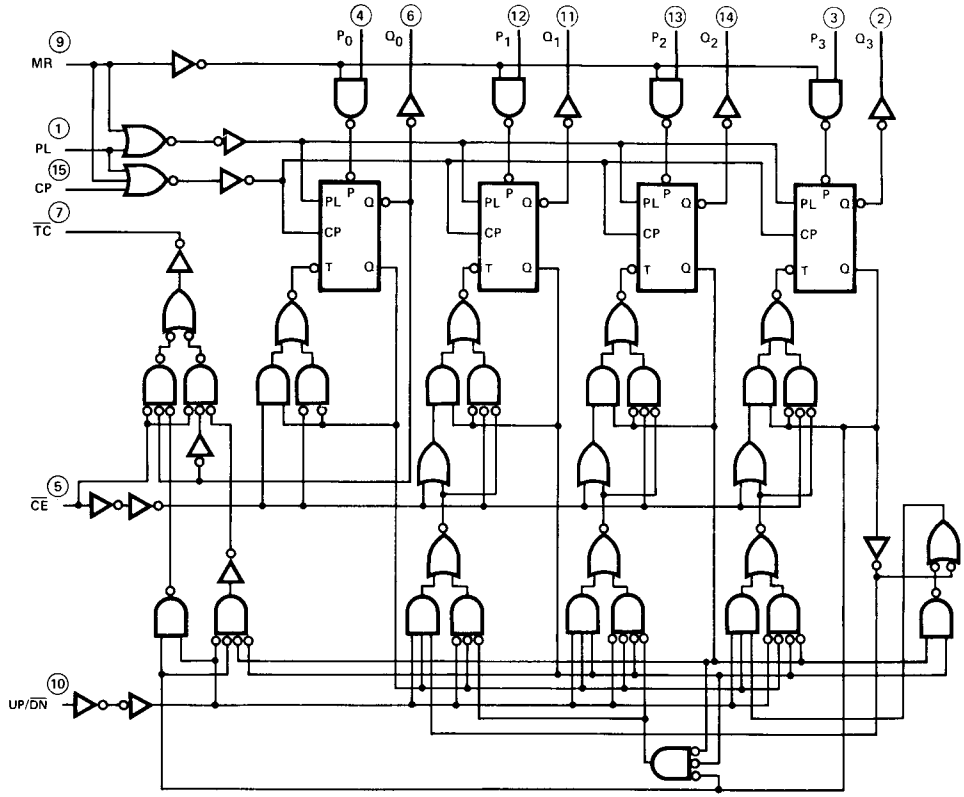
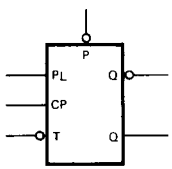
LOGIC DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 8
○ = Pin Number



PL (Parallel Load Input) — Asynchronously Loads P into Q, Overriding all Other Inputs
P (Parallel Input) — Data on this Pin is Asynchronously Loaded into Q, when PL is HIGH Overriding all Other Inputs
CP (Clock Pulse Input)
Q, Q̄ (True and Complimentary Outputs)
T (Toggle Input) — Forces the Q output to synchronously toggle when a HIGH is placed on this input.

DC CHARACTERISTICS: V_{DD} as shown, V_{SS} = 0 V (See Note 1)

SYMBOL	PARAMETER		LIMITS									UNITS	TEMP	TEST CONDITIONS
			V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15 V					
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
I_{DD}	Quiescent Power Supply Current	XC			20			40			80	μA	MIN, 25°C	All inputs at 0 V or V_{DD}
					150			300			600		MAX	
		XM			5			10			20	μA	MIN, 25°C	
					150			300			600		MAX	

Notes on folowing page.

AC CHARACTERISTICS AND SET-UP REQUIREMENTS: V_{DD} as shown, V_{SS} = 0 V, T_A = 25°C (See Note 2)

SYMBOL	PARAMETER	LIMITS									UNITS	TEST CONDITIONS
		V_{DD} = 5 V			V_{DD} = 10 V			V_{DD} = 15V				
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
t_{PLH}	Propagation Delay, CP to Q_n		150	350		62	160		41	128	ns	C_L = 50 pF, R_L = 200 kΩ Input Transition Times ⩽ 20 ns
t_{PHL}			150	350		59	160		39	128		
t_{PLH}	Propagation Delay, CP to $\overline{TC}$		167	450		71	180		48	144	ns	
t_{PHL}			252	650		100	245		66	196		
t_{PLH}	Propagation Delay, PL to Q_n		170	325		70	150		45	120	ns	
t_{PHL}			220	425		90	195		62	156		
t_{PLH}	Propagation Delay, MR to Q_n, $\overline{TC}$		225	500		170	210		105	168	ns	
t_{PHL}			205	450		120	190		80	152		
t_{TLH}	Output Transition Time		60	135		31	75		23	45	ns	
t_{THL}			65	135		25	75		18	45		
t_wCP	CP Minimum Pulse Width	125	50		60	21		48	14		ns	
t_wPL	PL Minimum Pulse Width	150	60		60	21		48	16		ns	
t_wMR	MR Minimum Pulse Width	150	60		60	30		48	20		ns	
t_{rec}	MR Recovery Time	175	75		70	30		56	20		ns	
t_{rec}	PL Recovery Time	150	62		60	24		48	17		ns	
t_s	Set-Up Time, UP/$\overline{DN}$ to CP	325	145		140	55		110	38		ns	
t_h	Hold Time, UP/$\overline{DN}$ to CP	0	-90		0	-35		0	-25			
t_s	Set-Up Time, $\overline{CE}$ to CP	275	118		120	49		96	33		ns	
t_h	Hold Time, $\overline{CE}$ to CP	0	-40		0	-15		0	-10			
t_s	Set-Up Time, P_n to PL	70	29		30	11		24	8		ns	
t_h	Hold Time, P_n to PL	0	-40		0	-20		0	-20			
f_{MAX}	Input Clock Frequency (Note 3)	2	5		5	12		6	15		MHz	

NOTES:
1. Additional DC Characteristics are listed in this section under 4000B Series CMOS Family Characteristics.
2. Propagation Delays and Output Transition Times are graphically described in this section under 4000B Series CMOS Family Characteristics.
3. For f_{MAX}, input rise and fall times are greater than or equal to 5 ns and less than or equal to 20 ns.
4. It is recommended that input rise and fall times to the Clock Input be less than 15 μs at V_{DD} = 5 V, 4 μs at V_{DD} = 10 V, and 3 μs at V_{DD} = 15 V.

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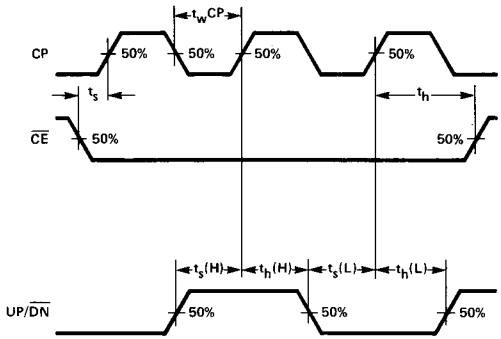
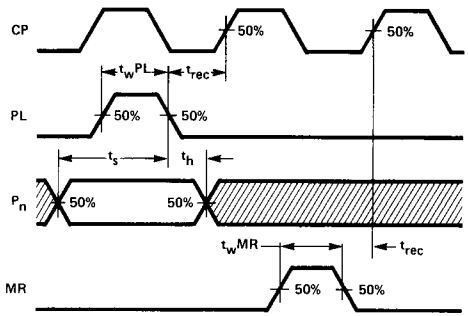
SWITCHING WAVEFORMS



MINIMUM CP WIDTH, SET-UP AND HOLD TIMES, $\overline{CE}$ TO CP AND UP/$\overline{DN}$ TO CP



MINIMUM PL AND MR PULSE WIDTH, RECOVERY TIME FOR PL AND MR, AND SET-UP AND HOLD TIMES, P_n TO PL

NOTE:
Set-up and Hold Times are shown as positive values but may be specified as negative values.